A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress

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ABSTRACT Based on the concept of switched-capacitor based multilevel inverter topology, a new structure for a boost multilevel inverter topology has been recommended in this paper. The proposed topology uses 11 unidirectional switches with a single switched capacitor unit to synthesize nine-level output voltage waveform. Apart from the twice voltage gain, self-voltage balancing of capacitor voltage without any auxiliary method along with reduced voltage stress has been the main advantages of this topology. The merits of proposed topology have been analyzed through various comparison parameters including component counts, voltage stresses, cost and efficiency with a maximum value of 98.3%, together with the integration of switched capacitors into the topology following recent development. Phase disposition pulse width modulation (PD-PWM) technique and nearest level control PWM (NLC-PWM) have been used for the control of switches. Different simulation and hardware results with different operating conditions are included in the paper to demonstrate the performance of the proposed topology.

INDEX TERMS Multilevel inverter, boost inverter topology, switched-capacitor, single dc source, reduce switch count, PWM.

I. INTRODUCTION

With the rapid growth of the renewable energy resources and its application in high voltage applications link industrial drive, high voltage dc transmission (HVDC), electric vehicle (EV), etc., power electronic converters play an important role in the power conversion suitable for each application. Multilevel inverters have their own importance in medium and high voltage applications due to reduced voltage rating of power semiconductor devices for high voltage generation, reduced harmonic contents, the small size of the filter, reduced EMI, improved efficiency and many more. Neutral point clamped (NPC), flying capacitor (FC) and cascade H-bridge (CHB) are traditional topologies that have been extensively researched and applied in different applications. However, the major concerns with these topologies have been the higher number of components, capacitor voltage balancing and complex control for a higher number of levels [1]–[4]. Therefore, numerous topologies have been proposed with reduce switch count [5]–[14]. In [7], an optimal design of multilevel inverter topology has been discussed. The topology of [7] uses several isolated dc voltage sources which restricts its applications. Another topology based on isolated voltage sources has been proposed in [9], in which 17 level...