Abstract: This study investigates the experimental validation of finite control set–predictive current control (FCS-PCC) of a multi-level four-leg voltage-source inverter (VSI) operating under balanced and unbalanced conditions. The proposed topology is a combination of conventional four-leg VSI with an additional four switches circuit serving as dc voltage synthesiser. Unified of both circuits can supply energy to unbalanced three-phase loads by providing the path for a zero-sequence load while maintaining appropriate load voltage to the system. The proposed control strategy takes advantage of the discrete nature of the power converter system to predict the future behaviour of the output current. FCS-PCC is based on an optimal approach that selects the most accurate switching signals among 48 valid switching states by computing cost function and applying switching state that minimises the tracking error to the next sampling time. The proposed control has been experimentally verified to assert the robustness of the control. The prominent outcomes of the experiments confirm the ability of independent load current reference tracking with harmonics distortion lower than the conventional eight switches VSI.

1 Introduction
The issue of unbalance load is highly related to power quality. In larger power systems, the load can exist in diverse nature, three phase, single phase, unbalance load and non-linear load. The unbalance loading condition can lead to instability and poor power quality. Conventional three phase, three-wire voltage-source inverter (VSI) is inappropriate for unbalanced load connection. For this VSI topology, it is not possible to independently track all the four filter currents. In actual implementation, when energy is supplied to a three-phase load, the risk of having an unbalanced load must be considered. If this case occurs, the power-conversion system must provide a path for the zero-sequence current to avoid system instability [1]. The four-leg topology is compatible with a diverse application such as active power filter [2], uninterruptable power supply, distributed power system [3] and rural electrification scheme where the arbitrary load is connected by the end user.

There are few topologies that can cater for unbalanced load conditions as described as [1, 4–9]. One of the simplest solutions is by employing split dc-link capacitor [7]. The excessive unbalance current is injected to split dc-link capacitor. It is only reliable to some extent of unbalance because the capacitors have limited voltage ripple tolerance [10]. When highly unbalance three-phase load is connected to this power circuit, the dc-link voltage significantly deviates from its optimal values. As a consequence, over-rated capacitors are designed for this purpose to withstand the neutral current flowing through them and to avoid sudden surge from destroying the dc-link capacitors. Thus, the volume of the power circuits increases and cost inefficient due to the price of the bulky capacitors. The midpoint of the split dc-link capacitor becomes the fourth wire of the converter, therefore utilised as the ground return. An alternative to split dc-link capacitor topology is the conventional VSI with Δ/Y or zig-zag transformer [7, 11–13]. The connection is performed by linking the delta winding to the inverter meanwhile the star winding to the load. The zero sequence current attenuation is achieved when the zero sequence current is trapped in the delta windings [14]. However, the central problem of this solution is the bulky size of the transformer. A low-cost and high-reliability alternative to this problem is to use a four-leg VSI at the load side, where the fourth leg serves a path for the zero-sequence current. This topology’s connection format is similar to the conventional three-phase inverter, except that it has an additional leg connected to the neutral point of the load, allowing for controllability of the zero sequence current/voltage [3]. As compared to other solution, the four-leg solution exhibits superior controllability because of the presence of additional leg. On the other hand, the four-leg VSI can handle the neutral current without affecting the capacitor life. Several technical issues discussed in the literature [15–17] related to this four-leg topologies are the substantial load current harmonics distortion.

The authors of [18] have successfully implemented the predictive current control for conventional four-leg VSI. Despite all the advantages of the predictive control, it has a significant shortcoming which is the variable switching frequency. This will lead to a wide spectrum of harmonics and increase the total harmonic distortion % (THD%) value. In effect, the experimental results of [9, 18] reveal substantial harmonics distortion for unbalance loading condition reaching up to 21.38% of distortion. Though, it is well-known fact that multi-level inverter topology is able to lessen the THD% values by selecting proper voltage level to the inverter.

The main contributions of this work are enlisted as follows:

i. The development of four-level four-leg VSI with minimum components count.
ii. Reduction of load current harmonics using newly developed topology.
iii. Conduct wide-ranging robustness test to experimentally validate the proposed topology.

This paper is organised as follows: Section 2 elaborates the mathematical modelling and analysis of the proposed multi-level four-leg VSI. Section 3 discusses the discrete mathematical model of the R–L load using forward Euler’s approximation. Section 4 presents the experimental results, and Section 5 recapitulates the research findings in the conclusion.

2 Multi-level four-leg VSI
The proposed topology multi-level inverter topology is a unification of conventional four-leg VSI with additional four switches circuit. The arrangement of the switching pairs ($S_i$, $S_j$) and
switching states of switch follows:

\[ V_{dc1} + V_{dc2} \]

Table 1 Switching state synthesising multi-level output

<table>
<thead>
<tr>
<th>( S_1 )</th>
<th>( S_2 )</th>
<th>( v_{PN} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>( V_{dc1} )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( V_{dc1} )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( V_{dc2} )</td>
</tr>
</tbody>
</table>

\( \{S_0, S_1\} \) resembles a synchronous buck converter without the reactive elements (Fig. 1). The proposed dual-buck circuit has three terminal input to accommodate the dual dc-link elements. The output terminal of the dual-buck topology is then able to synthesise multiple level of output voltage. One switch pair \( \{S_1, S_2\} \) is attached to the positive rail \( P \), and the other sub-circuit consisting of \( \{S_0, S_3\} \) is connected to the negative rail \( N \) to perform a symmetrical circuit with respect to the neutral point of the dual dc links \( V_{dc1} \) and \( V_{dc2} \). Both positive and negative rails are powered by a dual dc supply \( V_{dc1} \) and \( V_{dc2} \) respectively. The bar ‘\( \bar{x} \)’ denotes the complimentary switching states of switch \( S_x \), \( x \in \{1, \ldots, 6\} \). With regards to the dual-buck circuit, at any instant, only two switches are allowed to be switched ‘ON’. Therefore, following this constraint, there are four possible switching states. However, turning ‘ON’ \( \{S_0, S_3\} \) and \( \{S_1, S_2\} \) simultaneously may cause short circuit to the dc link and this configuration is restricted from the analysis. Table 1 recapitulates the allowable switching states of the dual asynchronous buck circuit.

From Table 1, it can be concluded that the output voltage \( V_{dc} \) can be generalised in a simple mathematical equation indicated as follows:

\[ v_{PN} = [S_0, S_3] \frac{V_{dc}}{V_{dc}} \quad (1) \]

In practical, \( V_{dc1} \) is set as the same value as \( V_{dc2} \). In this case, the resultant dc-link voltage \( V_{dc} = (V_{dc1} + 2V_{dc2}) \). Another method to increase the number of level is to set unequal dc-link voltage value. For example, \( V_{dc1} = 2V_{dc2} \). Therefore, \( V_{dc} = (V_{dc1} + 2V_{dc2} + 3V_{dc2}) \). It can be understood that this circuit can generate three non-zero values. The positive \( P \) and negative \( N \) terminals are attached to the conventional four-leg VSI to create a path for the zero-sequence current in case of unbalanced load. Each leg of the four-leg VSI operates as individual half-bridge inverter generating independent output from the dual dc-link voltage. Due to the binary nature of the switches and considering all four phases of the inverter, 16 valid switching possibilities can be counted. The zero-sequence current path is created by connecting the neutral point of the star connected the load to node \( d \) located at the fourth leg. By applying the Kirchhoff’s current law, it can be demonstrated that the neutral current can be expressed as

\[ i_n = -(i_a + i_b + i_c) \quad (2) \]

As the neutral of the load is directly connected to output phase \( d \), the load voltage of the inverter can be defined as the potential difference between the three-phase output nodes \( \{a, b, c\} \) to node \( d \). Mathematically, it can be expressed as

\[ v_d = \frac{V_{ad}}{V_{dc}} = \frac{S_1 - S_2}{S_1 - S_2} \frac{V_{dc1}}{V_{dc}} \quad (3) \]

The load voltage of the proposed multi-level and conventional four-leg VSI can be represented in \( a/β/γ \) reference frame as indicated in (4) and (5), respectively.

\[ \begin{bmatrix} \alpha \\ \beta \\ \gamma \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} & \frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} S_0 - S_3 \\ S_1 - S_2 \\ S_3 - S_1 \end{bmatrix} \frac{V_{dc1}}{V_{dc}} \quad (4) \]

\[ \begin{bmatrix} \alpha \\ \beta \\ \gamma \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{3}/2 & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} S_0 - S_3 \\ S_1 - S_2 \\ v_{PN} \end{bmatrix} \quad (5) \]

In the following analysis, sextuplet \( \{S_0, S_1, S_2, S_3, S_4\} \) denotes the switching states of the dual-buck circuit \( \{S_3, S_1\} \) and the four-leg VSI \( \{S_0, S_1, S_2, S_3\} \). Fig. 2 depicts the geometrical aspect of the load voltage in the \( a/β/γ \) reference frame using (4). The \( \alpha, \beta \) and \( γ \) are mutually orthogonal to each other. The voltage vectors form a three-dimensional hexagonal prism. With the integration of unequal dc-link voltages, the total number of voltage vectors populating the prism is tripled the number of voltage vectors of the conventional four-leg inverter.

Fig. 2 is plotted by considering \( V_{dc1} = 100 \text{ V} \) and \( V_{dc2} = 50 \text{ V} \). Fig. 2b illustrates the full construction of space voltage vectors for the proposed four-level four-leg VSI. The geometrical form resembles a hexagonal prism. As the input voltage is provided by the dual-buck circuit, three different levels can be considered. The immediate effect of the variable input voltage \( v_{PN} \) is the construction of hexagonal prism with different size and volume. The origin of the space vector is constructed by six sextuplets compared to two quadruplets for the conventional four-leg VSI.

The six sextuplets are a result of combination between three possible switching states of the dual-buck circuit \( \{S_0, S_3\} = \{(1, 1), (1, 0), (0, 1)\} \) and two switching states of the four-leg inverter \( \{S_0, S_1, S_2, S_3\} = \{(1, 1, 1), (0, 0, 0, 0)\} \). The remaining 42 sextuplets have unique space vector.
The sextuplets of the outer hexagonal prism (Fig. 2b) start with 11 which correspond to $V_{dc1} + V_{dc2}$. Meanwhile, the middle hexagonal prism has a smaller size and volume. The sextuplets which construct this hexagonal prism form start with 10 which correspond to an input dc-link equivalent to $V_{dc1}$ across the terminal $P$ and terminal $N$. Due to this reason, this hexagonal prism can be constructed with a scale $V_{dc1}/ (V_{dc1} + V_{dc2})$ of the full hexagonal prism indicated in Fig. 2b. For a better illustration of the middle hexagon, this geometrical figure has been zoomed as depicted in Fig. 2c. In a similar way, another hexagonal prism can be constructed by considering sextuplets starting with 01 as indicated in Fig. 2a.

The voltage space vector for the conventional four-leg inverter constitutes only the outer layer hexagonal prism without the middle and small hexagonal prism. It has seven layers on $\gamma$-axis (multiple of $V_{dc}/3$) [10]. On the other hand, for similar total dc-link voltage rating, it can be appreciated that the proposed multi-level unequal dc-link voltage topology has 13 layers on the $\gamma$-axis. Therefore, the voltage stress on the $\gamma$-axis has been reduced. As a consequence, load voltage with higher precision can be applied to the system compared to the conventional topology. With the integration of unequal dc-link voltages, the total number of voltage vectors populating the prism is tripled the number of voltage vectors of the conventional four-leg inverter.

Table 2 enlists the sextuplets of triangle $T_1$, $T_1'$ and $T_1''$. From Table 2, a clear relationship between $T_1$, $T_1'$ and $T_1''$ can be established. As an illustrative example, let us consider Fig. 3a. The extremity of the triangle $T_1$ represented by sextuplets (111110), (111100) and (110110). The last four components of the sextuplets remain similar for all $T_1$, $T_1'$ and $T_1''$. The only components which change are the first two digits $S_1$ and $S_2$ which describe the switching signal of the dual-buck circuit. By simultaneously switching ON $S_1$ and $S_2$, the dc-link generated by the dual-buck's output is equivalent to full $V_{dc}$ as indicated in Table 1. However, for $T_1''$, the first two digits are 10. Both configurations yield the same dc-link output value which equate $V_{dc}$. Similarly, $T_1''$ is constructed by considering $S_1 = 0$ and $S_2 = 1$.

Thus, it can be affirmed that $T_1$ and $T_1''$ are image projections characterised by centre at origin (0, 0, 0), scale factor of $V_{dc1} / (V_{dc1} + V_{dc2})$ and $V_{dc2} / (V_{dc1} + V_{dc2})$ of $T_1$ respectively. This analysis is valid for triangle $T_2$ as illustrated in Fig. 3d. Figs. 3c and 3d provide the sectional cut on the $\gamma$-axis of the proposed three-level four-leg VSI whereas Figs. 3a and 3b depict the view from the $\alpha = \beta$ plane. For the proposed multi-level circuit, both $\alpha$ and $\beta$ components are subdivided into six equidistance section. With six times smaller voltage steps on the $\alpha$ and $\beta$-axis, it is expected to synthesise load voltage with higher accuracy. In Figs. 3c and 3d, $d$ and $x$ denotes any possible values of the switching states, $x \in \{0, 1\}$.

3 Predictive current control

The predictive control technique offers an easy implementation for current control. On top of that, it can provide high accuracy, fast dynamic response and robust, throughout a wide range of operating conditions. The essence of model predictive control is the use of system's model to predict the future behaviour of the controlled variable by considering all valid switching states. The controller uses this information to compute a cost function representing the reference tracking error and other control requirements. In this case, the number of predictions is determined by the number of valid switching states of the converter. Finally, the selection of the optimal switching states is based on a predefined optimisation criterion at every predictive horizon. The flowchart in Fig. 4 briefly describes the predictive control scheme used in this paper.

Firstly, the control algorithm is initiated by acquiring basic measurements such as three phase load currents and voltages. In the same time, the reference values of load current are also generated. If relatively small sampling time is used, the generation of the reference load currents is straightforward. Nonetheless, if the sampling time is high, the reference values are obtained via Lagrange extrapolation technique to compensate the delay time [19].

Then, since the controller operates in discrete time, the analysis continues by developing a discrete model representing the input and output of the four-leg VSI. The same discrete model will be used to predict the behaviour of the output current. Euler's approximation method has been used to discretise the load currents. The continuous-time expression for the load current can be expressed as

Fig. 2 Three-dimensional voltage vectors for
(a) $V_{pn} = V_{dc1}$, (b) Full voltage vector of the proposed topology, (c) $V_{pn} = V_{dc2}$.
\[
d\begin{bmatrix} \dot{v}_o \\ \dot{i}_o \end{bmatrix} = \begin{bmatrix} \frac{1}{L_a} & 0 & 0 \\ 0 & \frac{1}{L_b} & 0 \\ 0 & 0 & \frac{1}{L_c} \end{bmatrix} \begin{bmatrix} v_{ad} \\ v_{bd} \\ v_{cd} \end{bmatrix} - \begin{bmatrix} R_a \\ R_b \\ R_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}
\]

\[
\frac{\dot{x}_o}{L} = \begin{bmatrix} \frac{1}{L_a} & 0 & 0 \\ 0 & \frac{1}{L_b} & 0 \\ 0 & 0 & \frac{1}{L_c} \end{bmatrix} \begin{bmatrix} v_{ad} \\ v_{bd} \\ v_{cd} \end{bmatrix} - \begin{bmatrix} R_a \\ R_b \\ R_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}
\]

where \( v_o = [v_{ad}, v_{bd}, v_{cd}]^T \) designates the three-phase voltage across the \( R - L \) load and \( i_o = [i_a, i_b, i_c]^T \) is the current flowing through the output phase. System's state \( v_o \) and controlled variable \( i_o \) are all made available by direct measurement from the system.

Knowing \( v_o \) and \( i_o \) at instant ' \( k \) ', it is possible to apply Forward Euler's to approximate the one step load current prediction as described by

\[
\begin{bmatrix} i_{a(k+1)} \\ i_{b(k+1)} \\ i_{c(k+1)} \end{bmatrix} = \begin{bmatrix} 1 - \frac{T_s R_a}{L_a} \\ 1 - \frac{T_s R_b}{L_b} \\ 1 - \frac{T_s R_c}{L_c} \end{bmatrix} \begin{bmatrix} i_{a(k)} \\ i_{b(k)} \\ i_{c(k)} \end{bmatrix} + \frac{T_s}{L} \begin{bmatrix} v_{ad(k)} \\ v_{bd(k)} \\ v_{cd(k)} \end{bmatrix}
\]

Finally, the predicted values defined earlier are applied to compute a cost function which deals with the control objective to choose the

\[\text{Fig. 3} \quad \text{Synthesis of the multi-level output voltage}\]

\[\text{Table 2} \quad \text{Relationship between triangle } T_1 \text{ and its image projections } T'_1 \text{ and } T''_1:\]

<table>
<thead>
<tr>
<th>Extremity</th>
<th>Sextuplet</th>
<th>Coordinate ((\alpha, \beta, \gamma)/V_{dc})</th>
<th>Sextuplet</th>
<th>Coordinate ((\alpha, \beta, \gamma)/V_{dc})</th>
<th>Sextuplet</th>
<th>Coordinate ((\alpha, \beta, \gamma)/V_{dc})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(110100)</td>
<td>(\left[\frac{1}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
<td>(100100)</td>
<td>(\left[\frac{2}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
<td>(010100)</td>
<td>(\left[\frac{1}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
</tr>
<tr>
<td>2</td>
<td>(111000)</td>
<td>(\left[\frac{2}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
<td>(101000)</td>
<td>(\left[\frac{2}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
<td>(011000)</td>
<td>(\left[\frac{1}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
</tr>
<tr>
<td>3</td>
<td>(110010)</td>
<td>(\left[-\frac{1}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
<td>(100010)</td>
<td>(\left[\frac{2}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
<td>(010010)</td>
<td>(\left[\frac{1}{3}, \frac{1}{\sqrt{3}}, \frac{1}{3}\right])</td>
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</tbody>
</table>
optimal switching states. In this project, the cost function incorporates two major objectives. The first objective is to remain exceptional load current reference tracking and to reduce the switching frequency of the fourth leg. The second control requirement is optional. $S_6$ and $S_{6o}$ bear higher switching frequency due to the regulation of zero-sequence current. As a consequence, the temperature of $S_6$ and $S_{6o}$ tend to increase rapidly and this will lead to short lifespan of the switches. Nonetheless, in this paper, the determination of weighting factor is not extensively studied and not the main objective of this paper. $g_i$ evaluates the load current deviation as given in the following equation:

$$g_i = \sum_{o \in [p, n, s]} |I_{lof}^{ref} - I_{lof}^o|.$$  

Equation (9) is a sub-cost function that penalises the switching state changes and $\lambda_{lof}$ is a weighting factor representing the degree of importance to the total cost function

$$g_t = \lambda_{lof} \left| S_{6o}^{ref} - S_{6o}^{o} \right|.$$  

Finally, the total cost function performing both control requirements is the sum of (8) and (9). The total cost function is computed 48 times in a repeated loop, and the switching combination that computes the minimum cost function will be applied to the next sampling time.

4 Results and discussion

In order to validate the stability and robustness of the proposed predictive current control scheme, an experimental four-level four-leg VSI prototype has been built in the laboratory. The control algorithm has been implemented using a reconfigurable Xilinx Spartan 6-LX45 FPGA (field-programmable gate array)-based controller. Twelve IRG30B120KD-E IGBT switches with ultra-fast recovery diode for the multi-level four-leg VSI are designed on a PCB board. Current sensor LEM LA25-NP and voltage transducers LEM LV-25-P are used to acquire the appropriate currents and voltages before sending to the ADC port of the FPGA. The scaling factor for the current and voltage transducers are fixed at 0.25 V/A and 0.005, respectively. The power circuit is powered by TDK Lambda dc power supply. The dc supply was tuned to 50 and 100 Vdc feeding the multi-level four-leg VSI. The digital output of the FPGA controller provides 12 gate drive signals by integrating sufficient dead-time to the complementary signal. The load current THD is measured using YOKOGAWA WT1800 Power Analyser. Fig. 5 illustrates the complete experimental setup of the project.

To validate the proposed control scheme, experimental testing has been conducted in various conditions such as steady state, transient state, balanced and unbalanced loads. The experimental parameters used during the experiments are enlisted in Table 3. In general, three sets of the test are conducted to assert the robustness of the control. Firstly, step change and frequency change test is conducted to observe the dynamic response of the measured load current against sudden changes of the reference amplitude and the reference frequency. After confirming the first test, the second test is carried out to evaluate the effect of three-phase unbalance loading condition. Finally, non-sinusoidal three-phase load current references are imposed to appraise the ability of the controller to track any signal as a reference.

4.1 Step change and frequency change test

The experimental conditions for this test are indicated as follows (Table 4):

Figs. 6a and b display the transient responses of the load current for abrupt reference amplitude and frequency change, respectively. With regard to the step change response, the measured load current is able to accurately track the new value within short transient period and nearly zero overshoot is recorded. The transient time is measured approximately around 2.4 ms. Meanwhile, the frequency change test inherits the same attribute as the step change test which maintains a very fast dynamic response. It is interesting to highlight that both dynamic responses are obtained without penalising the reference tracking ability.

The experiment for step change response test is repeated using three different power circuits corresponding to multi-level four-leg VSI with unequal dc-link voltage and equal dc-link voltage. The major difference between each topology is the number of output voltage levels. By introducing higher output level, the number of voltage steps increases and resulting higher accuracy output. Unlike the conventional circuit, regardless the load current demand, the output voltage always alternate between $-V_{dc}$, 0 and $+V_{dc}$ [20] as can be appreciated in Fig. 6d. Analysing Fig. 7, the transition from one level to another level occurs simultaneously without any intermediate undefined level. It can be explained by the fact that there is no switching occurs between non-adjacent levels.

4.2 Robustness test under balance and unbalance load conditions

The second test runs under the following conditions (Table 5) [1]:

Fig. 8a illustrates the experimental results for case 1. Case 1 represents the ideal condition where the load current reference and the load distribution are both balanced. All three-phase currents evolved sinusoidally following the same amplitude and frequency of the imposed references. Knowing that the load currents are balanced, the neutral current flows through the fourth leg converge towards zero. Fig. 8b shows the load current dynamic response of case 2. Here, different amplitude and frequency references are imposed to the system. The experimental result of case 2 reveals that independent load current tracking can be achieved. The load current on each output phase accurately following their respective reference regardless the difference in terms of amplitude and frequency. Due to the unbalance load currents, the neutral current which is the inverted sum of the three-phase currents, flows through the neutral connection. One interesting fact that can be deduced from this result is that the neutral current is not a pure sinusoidal due to the different frequency of load current. The
neutral current oscillates with two fundamental frequencies; 50 and 100 Hz. Therefore, during one complete cycle, two local maxima and two are corresponding to 50 and 100 Hz are observed.

Case 3 evaluates the behaviour of the load currents for balanced reference and unbalance loading condition. From Fig. 8c analogous load current waveforms as case 1 can be observed. In the same manner, the load current for case 4 nearly imitates the same feature as case 2 as shown in Fig. 8d. This is significant evidence that the unbalance loading condition is not penalising the reference tracking ability. However, both results differ in terms of current ripple. When connecting to unbalance loading condition, the load current ripple amplifies which contributes to slightly higher THD%. Another noticeable remark is that high value of inductive load current ripple amplifies which contributes to slightly higher THD%.

4.3 Non-sinusoidal reference test

The purpose of this test is to experimentally prove that predictive control is able to track non-sinusoidal references. Thus, two non-sinusoidal waveforms are set as a reference as listed below:

i. Three-phase triangular waveforms.
ii. Three-phase third harmonics sinusoidal waveforms.

Both references are characterised by a peak-to-peak value and frequency equal 4.0 A and 50 Hz, respectively. The results shown in Fig. 9 suggested that the proposed control is compatible to perform reference tracking of various kinds of waveforms.

In theory, model predictive current control is highly dependent on the load values. An interesting robustness test is tested to appraise the effect of model mismatch between the parameter given to the controller and the one applied to the load. In the following analysis, CL and CCL denote ‘changes to the load’ and ‘changes to the load and controller’. CL represents the model mismatch where the actual value of the load is not given to the controller. In this case, the controller only recognised the standard value of the load which is 24 Ω and 46 mH. On the other hand, CCL represents the case where the load parameters are changed and the controller parameters are modified according to the actual values of the loads.

Evaluation criterion of this test is the harmonics distortion. Resistive load ranging from 24 to 44 Ω with a step of 4 Ω and inductive load ranging from 46 to 66 mH with a step of 4 mH are considered for this test. The discrete values of THD% are extrapolated and represented in Figs. 10a and b. The case of model mismatch or CL recorded slightly higher distortion than the CCL. In the following analysis, CL and CCL denote ‘changes to the load’ and ‘changes to the load and controller’. CL represents the model mismatch where the actual value of the load is not given to the controller. In this case, the controller only recognised the standard value of the load which is 24 Ω and 46 mH. On the other hand, CCL represents the case where the load parameters are changed and the controller parameters are modified according to the actual values of the loads.

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4.4 Effect of λsw on load current THD and neutral current ripple

This section studies the effect of the λsw on the load and neutral current quality due to the optimisation condition given by (9). This optimisation is made by empirically adjusting λsw until an acceptable trade-off between the load current tracking and the switching frequency optimisation is met. Referring to (9), it can be understood that the rise of λsw will cause the cost function to prioritise switching frequency optimisation over the load current reference tracking. As a consequence, beyond the boundary limit of

Table 3 Parameters for experimental validation

<table>
<thead>
<tr>
<th>Designation</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td>resistive load R&lt;sub&gt;x&lt;/sub&gt;, R&lt;sub&gt;y&lt;/sub&gt;, R&lt;sub&gt;z&lt;/sub&gt;</td>
<td>24–44</td>
<td>Ω</td>
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<td>inductive load I&lt;sub&gt;x&lt;/sub&gt;, I&lt;sub&gt;y&lt;/sub&gt;, I&lt;sub&gt;z&lt;/sub&gt;</td>
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</tr>
<tr>
<td>load current I&lt;sub&gt;x&lt;/sub&gt;, I&lt;sub&gt;y&lt;/sub&gt;, I&lt;sub&gt;z&lt;/sub&gt;</td>
<td>1–2</td>
<td>A</td>
</tr>
</tbody>
</table>

Table 4 Parameters for step and frequency change

<table>
<thead>
<tr>
<th>Test</th>
<th>Reference amplitude, A</th>
<th>Reference frequency, Hz</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>step change</td>
<td>2 to 1</td>
<td>50</td>
<td>24 Ω, 46 mH</td>
</tr>
<tr>
<td>frequency change</td>
<td>2</td>
<td>50 to 25</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 5 Experimental setup
$\lambda_{sw} = 0.163$, the load current tracking performance will be deteriorated.

Figs. 11a and b illustrate the effect of the $\lambda_{sw}$ over the load current tracking by measuring the THD% of the load current for each phase and neutral current ripple amplitude, respectively. It

![Figures](image1.png)

**Fig. 6** Load current dynamic response for
(a) Step change, (b) Frequency change test, (c) Load voltage of the proposed topology, (d) Load voltage of the conventional four-leg inverter

![Figures](image2.png)

**Fig. 7** Zoomed view of $v_{ad}$

<table>
<thead>
<tr>
<th>Case</th>
<th>Phase</th>
<th>Reference amplitude, A</th>
<th>Reference frequency, Hz</th>
<th>Resistive load, $\Omega$</th>
<th>Inductive load, mH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>a</td>
<td>2</td>
<td>50</td>
<td>24</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>c</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>a</td>
<td>2</td>
<td>50</td>
<td>24</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>b</td>
<td>1</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>c</td>
<td>1</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>a</td>
<td>2</td>
<td>50</td>
<td>33</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>b</td>
<td></td>
<td></td>
<td>24</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>c</td>
<td></td>
<td></td>
<td>33</td>
<td>62</td>
</tr>
<tr>
<td>4</td>
<td>a</td>
<td>2</td>
<td>50</td>
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<td>46</td>
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<tr>
<td></td>
<td>b</td>
<td>1</td>
<td>50</td>
<td>24</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>c</td>
<td>1</td>
<td>100</td>
<td>33</td>
<td>62</td>
</tr>
</tbody>
</table>
appears that high $\lambda_{sw}$ are the causative factor of mediocre load current tracking performance as shown in Fig. 11a. Similarly, for $\lambda_{sw} \geq 0.08$, high neutral current ripple is recorded owing to high load current distortion.

Table 6 shows the numerical comparison between the proposed topology with alternative four-leg topologies available in the literature. In order to attain unbiased comparison, [9, 21] are based on the same predictive control. To recapitulate, it can be deduced that the unbalance load distribution generates uneven harmonics distributions. Thanks to the multi-level output voltage generating capability of the proposed topology, the current ripple is compensated by appropriately selecting suitable load voltage out of various values. Finally, the proposed topology with uneven dc-link voltage exhibits the best performance in terms of THD.

Fig. 8 Three-phase load current and zero sequence current for
(a) Case 1, (b) Case 2, (c) Case 3, (d) Case 4

Table 6 Quantitative comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>per phase THD%</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>a</td>
</tr>
<tr>
<td>case 1</td>
<td>4.31</td>
<td>4.38</td>
<td>4.56</td>
<td>4.21</td>
</tr>
<tr>
<td>case 2</td>
<td>4.21</td>
<td>4.97</td>
<td>5.02</td>
<td>4.18</td>
</tr>
<tr>
<td>case 3</td>
<td>4.28</td>
<td>4.65</td>
<td>4.60</td>
<td>4.32</td>
</tr>
<tr>
<td>case 4</td>
<td>4.19</td>
<td>5.20</td>
<td>5.25</td>
<td>4.37</td>
</tr>
<tr>
<td>number of levels</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>number of switches</td>
<td>12 IGBTs</td>
<td>12 IGBTs</td>
<td>8 IGBTs</td>
<td>16 IGBTs8 diodes</td>
</tr>
<tr>
<td>number of dc-link source, s</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>number of iterations</td>
<td>48</td>
<td>48</td>
<td>16</td>
<td>81</td>
</tr>
</tbody>
</table>

Fig. 9 Measured load current resulting from
(a) Triangular waveform, (b) Sinusoidal waveform with third harmonics injection

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In this paper, model predictive control is considered for controlling the switching states that minimise the cost function. The tests have been conducted at the laboratory level. The predictive output voltages by setting unequal dc-link values. In order to synthesise four-level output voltages are via additional four switches circuit.

This topology requires only two dc-links to synthesise four-level current control evaluates 48 possible switching combinations and the load current for a multi-level four-leg VSI. The multi-level experimental results reveal that the proposed control scheme is able to accurately track arbitrary reference.

6 References


[8] Roberto, C.: ‘3D-SVM algorithm and capacitor voltage balancing in a 4-leg NPC converter operating under unbalanced and non-linear loads four-leg NPC inverter space vector modulation (SVM) for a four-leg NPC inverter’. 15th European Conf. on Power Electronics and Applications (EPE), Lille, France, 2–6 September 2013, pp. 1–10


