An Improved Discontinuous Space Vector Modulation for Z-source Inverter with Reduced Power Losses

Ibtissam Chaib, Student Member, IEEE, El Madjid Berkouk, Jean-Paul Gaubert, Member, IEEE, Mostefa Kermadi, Member, IEEE, Nassereddine Sabeur, and Saad Mekhilef, Senior Member, IEEE

Abstract—This paper proposes a control strategy for a three-phase Z-source inverter using a modified discontinuous space vector modulation. The main advantages of the proposed control strategy are the enhanced output power quality and the compromise in the reduction between conduction and switching losses. Furthermore, the reduced switching losses are achieved by the elimination of one switching transition in each half sector with a proper selection of the shoot-through state distribution. In addition, the reduced conduction losses are achieved by dividing all sectors equally into 30°. MATLAB/SIMULINK simulation is carried out to verify the effectiveness of the proposed control strategy and compare it with the existing space vector modulation techniques that utilize distributions of four and six shoot-through vectors. PLECS software is used for conduction and switching losses calculation. Compared to the other modulation techniques, the key features of the proposed control strategy are the improved boosting capability of the output voltage, the low total harmonic distortion, the reduced conduction and switching losses, and the reduced inductance current ripple. An experimental test-bench that comprises of a three-phase Z-source inverter feeding an R load, controlled by a dSPACE MicroLabBOX, is used to verify experimentally the effectiveness of the proposed control strategy. It is envisaged that the proposed control strategy can be very useful for electrical drive applications integrating three-phase Z-source inverter due to its capability to improve the output waveform and reduce the harmonic distortions, switching and conduction losses.

Index Terms—Z-source inverter, space vector, pulse width modulation, shoot-through control, Discontinuous Space Vector Modulation.

I. INTRODUCTION

In power conversion systems, the traditional inverter can provide only buck output voltage and its maximum output voltage cannot exceed the dc-link voltage. In two-level inverters, the upper and the lower power switch of each phase leg cannot be turned on at the same time. Otherwise, shoot-through would occur and the power semiconductor switching devices will be destroyed. To overcome such limitations, several recent research studies proposed different improved inverter topologies. One of them is the Z-source inverter proposed by Peng [1].

The Z-source inverter uses an impedance network (Z-network), to replace the traditional dc link. It employs an impedance network, that consists of split-inductors L1 and L2 and capacitors C1 and C2 connected in an X shape. It couples the inverter to the dc source, load, or another converter. Therefore, the dc source can be a battery, a diode rectifier, thyristor converter, fuel cell, an inductor, a capacitor, or a combination of those [1]. Compared to the conventional two-level three-phase inverter which has six active vectors and two zero vectors, the commutation cell of the two-level three-phase Z-source inverter bridge has one extra state, called the shoot-through state. This state can be generated when both switches of any one phase leg are gated on. This state can be generated in seven different ways: shoot-through via any one phase leg, combinations of any two-phase legs, and all three-phase legs. The Z-source inverter advantageously uses the shoot-through states to buck and boost the dc bus voltage to the desired output voltage. The equivalent circuit and the model of the Z-source inverter have been studied in [1]. The Z-source inverter is recently integrated into a wide range of applications: in electrical and hybrid vehicles [2-4], in renewable power generation systems such as photovoltaic systems [5-9], wind turbine systems [10-12]. Furthermore, the Z-source inverter is used as a multilevel inverter in [13-15].

To control the duty cycle of the shoot-through, researchers investigated several modified and space vector pulse width modulation (SVPWM) techniques [16]. In conventional carrier-based PWM methods, the switching sequence is modified by introducing the shoot-through into the vectors state without compromising the active states. Hence a several modified PWM were proposed: simple boost control [1], maximum boost control [17], constant boost control [18] and maximum constant boost control [19]. Each strategy has its advantages and inconveniences that were discussed and compared in terms of switching losses, current ripple, total harmonic distortion THD and boosting ability in [16, 20, 21]. However, the major common drawback in all the above-mentioned strategies is the
fact that the generation of the shoot-through can be occurred by
the combination of the three legs, which increases the switching
losses, although the shoot-through can be generated only by one
leg. To overcome the limitations of modified PWM, authors in
[22] proposed a modified space vector PWM (SVPWM) for the
Z-source inverter, in which the shoot-through can be generated
by using only one leg. As highlighted in [23], the SVPWM is
easy to implement and has better performance than the modified
PWM with reduced total harmonic distortion and lower current
ripple. The modified SVPWM for Z-source inverter (ZSVPWM) gives the possibility to find the best distribution of
the shoot-through state between the vectors state to reduce the
switching losses by using only one switch in each transition.
Hence, many ZSVPWMs have been developed to control the
duty ratio of the shoot-through [24-26]. In recent literature,
ZSVPWM techniques with four shoot-through vectors distribution (4-ZSVPWM) and 6 shoot-through distribution (6-
ZSVPWM) were presented in [27, 28], and in [29], respectively. Both 4-ZSVPWM and 6-ZSVPWM have 12
switching transitions. The advantage of the 6-ZSVPWM is that
it uses only one leg to generate the shoot-through in each
switching cycle while the 4-ZSVPWM uses two legs separately
to generate the shoot-through state for each switching cycle. Despite having high performance, ZSVPWMs suffer from
minimal power transfer due to the utilization of zero voltage
vectors (000) and (111) in all sectors. In addition, ZSVPWM
suffers from high THD since all the switches have at least two
transitions in each switching cycle [30]. To enhance the
switching losses, researchers proposed the discontinuous Space
Vector pulse width modulation D-ZSVPWM for the Z-source
inverter in [30-32]. Despite the efficiency of the D-ZSVPWM
in terms of reducing the switching losses and maximizing the
power transfer, the conduction losses are appeared to be a
challenging problem. This is due to holding on the switches in
full conduction throughout the 60° interval [33].

To overcome the above-mentioned limitations, this work
proposes an improved discontinuous space vector pulse width
modulation (ID-ZSVPWM) to control the Z-source inverter. To
reduce the conduction losses and maintain low switching losses,
each sector 60° is split by two, thus dividing the alpha-beta plane
by 12 sectors of 30°. By doing so, the switches stay in full
conduction only for 30° instead of 60°. In the proposed ID-
ZSVPWM, the shoot-through states are introduced without
compromising the active states or affecting the invariable
switches in each switching cycle. The proposed ID-ZSVPWM
has the following merits: 1) enhanced output waveforms quality
and reduced THD due to the wise vectors’ distribution, 2)
reduced conduction losses due to the sectors divisions into
subsectors, and 3) ensured maximum power transfer is
guaranteed due to the minimal use of the zero states. The
effectiveness of the proposed control strategy is verified
through simulation using MATLAB/SIMULINK and PLECS
software. Besides, an experimental test is carried out using a
reduced scale Z-source inverter laboratory prototype controlled
by dSPACE MicroLabBOX to validate the simulation.

The remainder of this paper is organized as follows: Section
II presents a brief description of the Z-source inverter (ZSI). In
Section III, ZSVPWM with of 4 and 6 shoot-through states
distributions are reviewed. The proposed DZSVPWM is
described in Section IV. Comparative simulation with 4-
ZSVPWM and 6-ZSVPWM is made in Section V. Hardware
results and discussions are presented in Section VI. The
conclusion is presented in Section VII.

II. THE Z-SOURCE INVERTER

Fig. 1 shows the topology of the Z-source inverter. It
consists of an impedance network: inductors L1 and L2 and
capacitors C1 and C2 connected in X shape linked with a dc
source. The impedance network is feeding a three-phase
inverter. The latter supply a resistive load through an LC filter.
The Z-source inverter has two main operating modes, shown in
Fig. 2. Fig. 2(a) shows the equivalent circuit during the shoot-
through state where the upper and the lower switches of any
legs are turns on. Q represents the equivalent switch during the
shoot-through state. Fig. 2(b) shows the equivalent circuit
during the non-shoot-through state where the inverter bridge
works as a traditional inverter [1].

As verified in detail in [1], the basic principle relationship
for ZSI is:

\[ V_{c1} = V_{c2} = V_c = \frac{1-d}{1-2d} V_{dc}, d = \frac{T_{sht}}{T} \]  

(1)

Where

\[ V_l = \frac{1}{1-2d} V_{dc} = BV_{dc} \]  

non shoot−through state

(2)

\[ V_l = 0 \]  

shoot−through state

(3)

where \( V_{c1} \) and \( V_{c2} \) are capacitors voltage of impedance network
which are the same due to circuit symmetry. B is the boost
factor of ZSI. \( V_{dc} \) and \( V_l \) denote the input and output voltages
of impedance network respectively. \( d \) is the shoot-through duty
ratio \( d = T_{sht}/T ; T_{sht} \) is the total shoot-through time interval; \( T \)
is the control cycle.

![Fig. 1. Block diagram of the Z-source inverter.](image1)
![Fig. 2. Equivalent circuits of the Z-source inverter:](image2)

(a) shoot-through state

(b) Non shoot-through state.
III. CONVENTIONAL Z-SOURCE SPACE VECTOR PULSE WIDTH MODULATION ZSVPWM

The traditional SVPWM is defined by eight (8) vectors, six (6) active vectors and two (2) zero vectors. The active vectors divide the space vector plane into six (6) equal magnitude sectors, as shown in Fig. 3. The magnitudes are normalized with respect to the dc bus voltage $V_{dc}$ [34]. The time interval of the active and the zero vectors can be defined as [35] [36]:

$$
\begin{align*}
T_1 &= T_s r \sin \left[ \frac{\pi}{3} - \theta + \frac{\pi}{2} (i-1) \right] \\
T_2 &= T_s r \sin \left[ \frac{\pi}{2} (i-1) \right] \\
T_0 &= T_s - T_1 - T_2
\end{align*}
$$

(4)

$T_1$, $T_2$, and $T_0$ are the time intervals of the active vectors, the zero vector, and the time interval of the zero vector, respectively. $T_s$ is the switching period. $r$ is the modulation index.

$T_1$, $T_2$, and $T_0$ are equally divided into six (6) parts per control cycle as shown in Fig. 3 [29].

IV. PROPOSED ID-ZSVPWM

The proposed ID-ZSVPWM aims to reduce the total harmonic distortion of the output signal by and compromise between the conduction losses reduction and the reduction of switching losses. This objective is achieved by the elimination of one switching transition in each half sector for 30° with a proper selection of the shoot-through state distribution. In this strategy, each sector is divided into two sub-sectors. Hence the number of sectors becomes 12 sectors of 30° for each one as shown in Fig. 5 [29].

$$
d_{\text{max}} = \left( \frac{T_0}{T_s} \right)_{\text{min}} = 1 - r
$$

(9)

By replacing (7) in (8), $d_{\text{max}}$ can be rewritten as follows:

$$
d_{\text{max}} = 1 - \frac{\sqrt{3}}{2} m
$$

(10)

The boosting factor, denoted by $B$, is calculated using the following equation:

$$
B = \frac{1}{\sqrt{3} m - 1}
$$

(11)

Due to the significant capabilities of the implementation of the SVPWM in discrete systems, it has been widely used for the Z-source inverter. Therefore, researchers modified the SVPWM by introducing the shoot-through states into the zero vectors without compromising the active states. Two main control strategies were proposed in the literature: 4-ZSVPWM where the desired total shoot-through time interval is equally divided into four (4) parts per control cycle as shown in Fig. 4 [27]. 6-ZSVPWM where the desired total shoot-through time interval is equally divided into six (6) parts per control cycle as shown in Fig. 5 [29].
Fig. 6. Each subsector has only one zero vector either $V_0(000)$ or $V_1(111)$ at the beginning or the end of each switching sequence. Table 1 list the switching sequence of the proposed ID-ZSVPWM and the switching sequence of the conventional Z-source SVPWM.

<table>
<thead>
<tr>
<th>Sector</th>
<th>Conventional sequence</th>
<th>ID-ZSVPWM sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
</tr>
<tr>
<td>II</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
</tr>
<tr>
<td>III</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
</tr>
<tr>
<td>IV</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
</tr>
<tr>
<td>V</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
</tr>
<tr>
<td>VI</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
<td>$(V_0V_2V_4, V_0V_2V_4)$</td>
</tr>
</tbody>
</table>

Unlike in the conventional Z-source SVPWM the shoot-through state is distributed properly in the proposed ID-ZSVPWM, without changing the state of the maintained switches in each switching cycle. Table 2 lists the switching sequence and the distribution of the shoot-through state in each subsector for a half switching cycle. Four shoot-through states are inserted in each switching cycle without affecting the active states with a duration of $T_{sh}/4$ without affecting the active states. The proposed switching sequence for the ID-ZSVPWM for the first sub-sector is shown in Fig. 7(a) and Fig. 7(b) respectively, as shown in Fig. 7, in the first sub-sectors $S_3$ is maintained off and $S_6$ is maintained on. In the second sub-sector, $S_1$ is maintained on and $S_8$ is maintained off. And this procedure repeats in each sub-sector (30°) for different legs. This procedure ensures the reduction of conduction losses and maintain lower switching losses.

V. RESULTS & DISCUSSION

To evaluate the performance of the proposed ID-ZSVPWM strategy, simulation using Matlab/SIMULINK software and experiment are carried out. As shown in Fig.8, the system consists of a Z-source inverter linked with a dc source, feeding a three-phase resistive load through an LC filter. The main parameters of the described system are listed in Table 3. This simulation aims to compare the proposed strategy with 4-ZSVPWM and 6-ZSVPWM, in term of the dc-bus voltage boosting, and the current and voltage THD reduction. The obtained simulation results are listed in Table 4. The simulation results in continuous time mode for the 4-ZSVPWM, 6-ZSVPWM, and ID-ZSVPWM, are plotted in Fig. 9, Fig. 10 and Fig. 11 respectively, where the inverter dc-bus $V_i$, the Z-source capacitor voltage $V_c$, and the input DC-source voltage $V_{dc}$ are plotted in figure part (a), the inductance current $I_l$ is shown in figure part (b), and the current and voltage output FFT analysis are shown in figure parts (c) and (d) respectively.

For $V_{dc}=10$ V, $d=0.3$ and a modulation index $m=0.8$, the boost factor for 4-ZSVPWM is equal to $B_{4-ZSVPWM} = 1.9$ and the $THD_{4-ZSVPWM} = 0.74\%$ as shown in Fig. 9. Although, for the 6-ZSVPWM strategy, the boost factor is increased to $B_{6-ZSVPWM} = 2.54$, and the THD is reduced $THD_{6-ZSVPWM} = 0.7\%$ as shown in Fig.10, the proposed strategy shows better results. Where the boost factor is increased to $B_{ID-ZSVPWM} = 2.6$, with an improved $THD_{ID-ZSVPWM} = 0.17\%$ as shown in Fig.11 The current output THD and the voltage output THD show the same patterns due to the resistive load.
The proposed ID-ZSVPWM has the highest boost factor $B_{\text{ID-ZSVPWM}} = 2.6$, the lowest total harmonic distortion, and an acceptable inductance current ripple $\Delta I_d = 0.325A$. Thus, the proposed ID-ZSVPWM outperforms the other methods in terms of 1) enhancing the signal quality of the ac output voltage waveform (reduced THD), 2) ensuring the highest boost factor of the dc-link voltage, and 3) maintaining a good current ripple in the inductance.

In addition, the zoomed waveform of $V_{\text{dc}}$, resistive load voltage $V_{\text{res}}$, the line to line voltage $V_{\text{L}}$, and the inductor current $I_L$ within five (5) control cycles ($2e^{-3}$ s) are plotted in Fig. 13 (c). It can be seen from Fig. 13(a) and Fig. 13(b) that the ID-ZSVPWM present a small current inductor ripple value $\Delta I_{L_{\text{Id-ZSVPWM}}} = 0.47A$. Beside the voltage $V_i(t)$ equals to 16.5V, the voltage $V_c(t)$ equals 13.9V, resulting in a boost factor equals to 1.65. The digital controller successfully generates the appropriate switching gate signals to achieve the desired output waveform. From the waveforms of Fig. 13(c), it can be seen that the switching sequence presented in Fig. 7 is successfully generated using the ID-ZSVPWM. The distribution of the ST into four periods per control cycle appears in the experimental waveforms, and $V_i$ becomes zero and $I_L$ increases during ST periods. The measurement of the AC-Bus (the current load $I_{\text{load}}(A)$, the line to line voltage $V_{\text{ab}}(v)$, the phase voltage $V_{\text{an}}(v)$, resistive load voltage $V_{\text{res}}(v)$) are presented in Fig. 13(d), where the voltage across the resistor is $V_{\text{res}} = 10V$, the phase voltage is $V_{\text{an}}(v) = 12.8V$. Hence, the inverter factor is $G = 1.28$ which is nearly equal to the theoretic value. The simulation and experimental results are similar, which validate the performance of the proposed control scheme.

### TABLE 2

<table>
<thead>
<tr>
<th>Sector</th>
<th>subsector</th>
<th>switches</th>
<th>$T_0$</th>
<th>$T_{1n}$</th>
<th>$T_1$</th>
<th>$T_{2n}$</th>
<th>$T_2$</th>
<th>$T_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>(V_{1c}V_{1b}V_{2b}V_{2c}V_{0})</td>
<td>$S_1(S_2S_3)$</td>
<td>111</td>
<td>111</td>
<td>110</td>
<td>110</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>II</td>
<td>(V_{1c}V_{1b}V_{2b}V_{2c}V_{0})</td>
<td>$S_3(S_2S_3)$</td>
<td>111</td>
<td>111</td>
<td>110</td>
<td>110</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>III</td>
<td>(V_{1c}V_{1b}V_{2b}V_{2c}V_{0})</td>
<td>$S_2(S_3S_4)$</td>
<td>000</td>
<td>001</td>
<td>001</td>
<td>001</td>
<td>011</td>
<td>011</td>
</tr>
<tr>
<td>IV</td>
<td>(V_{1c}V_{1b}V_{2b}V_{2c}V_{0})</td>
<td>$S_2(S_3S_4)$</td>
<td>111</td>
<td>111</td>
<td>101</td>
<td>101</td>
<td>001</td>
<td>001</td>
</tr>
<tr>
<td>V</td>
<td>(V_{1c}V_{1b}V_{2b}V_{2c}V_{0})</td>
<td>$S_2(S_3S_4)$</td>
<td>000</td>
<td>010</td>
<td>010</td>
<td>010</td>
<td>110</td>
<td>110</td>
</tr>
<tr>
<td>VI</td>
<td>(V_{1c}V_{1b}V_{2b}V_{2c}V_{0})</td>
<td>$S_2(S_3S_4)$</td>
<td>000</td>
<td>001</td>
<td>001</td>
<td>001</td>
<td>011</td>
<td>011</td>
</tr>
</tbody>
</table>

To validate the proposed strategy experimentally, a prototype of Z-source inverter feeding a three-phase resistive load through an LC filter was built as shown in Fig. 12. The operation parameters used in the simulation and listed in Table 3 are used for the experiment. A Chroma 62150H-600S/1000S Solar Array Simulator was used as a dc power supply. The proposed ID-ZSVPWM strategy is implemented through a dSPACE MicroLabBOX controller. The dSPACE MicroLabBOX controls the switches through an IGBT Driver SKHI 23/12 (R) with a switching frequency equals to $f_{\text{sw}} = 2.5$ kHz and a sampling time equal to $f_s = 25$ kHz.

The obtained experimental results are listed in Table 5 for a modulation index $m = 0.8$ and a duty cycle equal to $d = 0.3$, as shown in Fig. 13. The measurement of the dc-Bus ($V_{dc}(v)$, $V_c(v)$, $V_L(v)$; $I_L(A)$) are presented in Fig. 13 (a) and Fig. 13 (b).

### TABLE 3

<table>
<thead>
<tr>
<th>$V_{dc}$</th>
<th>$m$</th>
<th>$d$</th>
<th>$C_s$</th>
<th>$I_{sw}$</th>
<th>$I_L$</th>
<th>$L_f$</th>
<th>$C_f$</th>
<th>$R_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 V</td>
<td>0.8</td>
<td>0.3</td>
<td>5mH</td>
<td>3.3mF</td>
<td>2.5 kHz</td>
<td>25 kHz</td>
<td>20mH</td>
<td>110Ω</td>
</tr>
</tbody>
</table>

Fig. 8. Complete block diagram of Z-source system.
Fig. 9. 4-ZSVPWM Simulation results (a) $V_{dc}(v)$, $V_{c}(v)$, $V_{i}(v)$ voltages; (b) inductance current $I_L(A)$; (c) current FFT analysis; (d) voltage FFT analysis.

Fig. 10. 6-ZSVPWM Simulation results (a) $V_{dc}(v)$, $V_{c}(v)$, $V_{i}(v)$ voltages; (b) inductance current $I_L(A)$; (c) current FFT analysis; (d) voltage FFT analysis.

Fig. 11. ID-ZSVPWM Simulation results (a) $V_{dc}(v)$, $V_{c}(v)$, $V_{i}(v)$ voltages; (b) inductance current $I_L(A)$; (c) current FFT analysis; (d) voltage FFT analysis.
PLECS software is used to measure and compare the conduction and switching losses dissipated by the six switches IGBT 1KQ120N60T in the steady-state for a rated power of 3 kW. For each strategy, the measurements are taken for a different modulation index values [0.7-1.1] as shown in Fig.14. The measurement of switching losses, conduction losses, and total power losses are shown in Fig. 14(a), Fig. 14 (b), and Fig. 14 (c), respectively. It can be concluded from Fig. 14(c) that the power losses increase with the rise of the modulation index in all three strategies. This can be attributed to the increase of power transfer with the height of $T_1$ and $T_2$. Furthermore, the rate of power losses for high modulation index are 8.83%, 9.54% and 6.33% for 4-ZSVPWM, 6-ZSVPWM, and ID-ZSVPWM, respectively. As can be seen from the analysis of the power losses, the proposed ID-ZSVPWM ensures the lowest power losses rate for high modulation index. At $m=0.7$, the power losses of ID-ZSVPWM equals 118.82W while for 4-ZSVPWM, it equals 106.52W. Hence, the losses of 4-ZSVPWM are 10.36% less than that of using ID-ZSVPWM. Nevertheless, the values are very close to each other. However, for a higher modulation index, the advantages of the proposed in reducing the power losses appear. If we take $m=1.1$, the power losses of the proposed ID-ZSVPWM is lower by 28.28% than that achieved using 4-ZSVPWM.

The power loss of the inverter main bridge as a function of switching frequency for $m = 0.8$ and $d = 0.3$ is plotted in Fig. 15. The switching losses increase when the switching frequency increases and becomes significant after 20 kHz for all the strategies. Besides, 6-ZSPWM has the highest switching losses due to the number of transitions per control cycle (6 times shoot-through), 4-ZSPWM and the ID-ZSPWM have a close dissipated power with a better performance of the proposed strategy. Moreover, Fig. 15(a) shows that the conduction losses are almost constant for all the strategies regardless the changing the switching frequency. This means that the changing of the switching frequency changes only the switching losses and has no influence on the conduction losses. The results show that beyond all the cited strategies, the ID-ZSPWM is the best compromise between switching losses and conduction losses, without reducing the signal output quality especially for the high modulation index, which confirms the efficiency of the proposed strategy.

TABLE 5

<table>
<thead>
<tr>
<th>EXPERIMENTAL RESULTS</th>
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<tbody>
<tr>
<td>$G$</td>
</tr>
<tr>
<td>$B$</td>
</tr>
<tr>
<td>$V_a$ (V)</td>
</tr>
<tr>
<td>$V_i$ (V)</td>
</tr>
<tr>
<td>$V_{Res}max$ (V)</td>
</tr>
<tr>
<td>$V_{an}max$ (V)</td>
</tr>
<tr>
<td>$V_{ab}max$ (V)</td>
</tr>
<tr>
<td>$I_{loadmax}$ (A)</td>
</tr>
<tr>
<td>$I_{in}$ (A)</td>
</tr>
<tr>
<td>$I_{Lmin}$ (A)</td>
</tr>
<tr>
<td>$\Delta I_L$ (A)</td>
</tr>
<tr>
<td>$\Delta I_L/I_L$</td>
</tr>
</tbody>
</table>

The power loss of the inverter main bridge as a function of switching frequency for $m = 0.8$ and $d = 0.3$ is plotted in Fig. 15.
VI. CONCLUSION

In this investigation, the aim is to assess a new proposed strategy, for the three-phase Z-source inverter named ID-ZSVPWM. The most challenging problem in the control strategy for the Z-source inverter is to provide a good signal quality with reduced power losses. The proposed ID-ZSVPWM reduces the conduction losses and maintains lower switching losses by 1) the division of each sector to two subsectors of 30°, 2) maintaining two switches of one leg (one is on while the other is off) in the steady-state of each subsector, and 3) with wise distribution of four (4) shoot-through state in the switching period. The ID-ZSVPWM has been compared with the 4-ZSVPWM and 6-ZSVPWM strategies, it has been shown from MATLAB simulation, PLECS measurements and experimental results that the proposed ID-ZSVPWM strategy has lower conduction losses, lower switching losses for the high modulation index, and has a lower current/voltage THD, lower current ripple in the inductors, and higher boost factor.

ACKNOWLEDGMENT

The authors would like to thank National Polytechnic School of Algiers (ENP), Algeria and University of Malaya, Malaysia, for providing financial support under Impact Oriented Interdisciplinary Research Grant (IIRG): IIRG011A-2019, and Ministry of Higher Education, Malaysia under Large Research Grant Scheme (LRGS): LR008-2019.

REFERENCES


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