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# Lanthanide rare earth oxide thin film as an alternative gate oxide

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ABSTRACT

An ultrathin gate oxide is needed for future nanoscale technology due to the density of integrated circuits will increase exponentially every two to three years as predicted by Moore's Law. Some problems were occurred in conventional silicon dioxide gate oxide during applications such as high leakage current density, low reliability issues, and undesirable power dissipation. Lanthanide rare earth oxides was attracted as one of potential candidates to replace conventional silicon dioxide due to their superior properties. Each rare earth oxides in lanthanide group was reviewed and discussed in terms of physical, chemical, and electrical properties and also its common deposition methods. $Sm_2O_3$ is one of the promising candidate materials among rare earth oxides because of some outstanding properties such as high κ (7–22), high breakdown electric field (5–7 MV $cm^{-1}$), relatively large bandgap (4.33 eV), low leakage current, large conduction offset with Si, high thermal stability, small frequency dispersion, low trapping rate, and low hygroscopic characteristic. The literatures of $Sm_2O_3$ was paid particular attention in the last section. The previous deposition methods of the $Sm_2O_3$ as gate oxide were reviewed and compared.

## 1. Introduction

As predicted by Moore's Law, the density of integrated circuit and the number of devices will increase exponentially and double every two to three years [1–6]. This significant development of technology requires ultrathin gate oxide (~ 1.5 nm or 4 atomic layers) of silicon dioxide ($SiO_2$) layer [1,3,7,8]. An extremely thin film may lead to large leakage current density owing to large amount of quantum-mechanical tunneling through the gate oxide and low reliability of gate oxide against the electrical breakdown [1,3,7]. This may cause unacceptable static power dissipation in the device [1,3,9]. The gate leakage problem occurred since late 1990s [2,3,10,11]. However, this problem is not solved completely even though enormous ingenuity and efforts were done by numerous researchers due to continued downscaling trend. For CMOS technology, a specific gate capacitance was designed to be proportional to the dielectric constant (κ) and inversely proportional to the thickness of the gate oxide [1,12]. For the sake of reducing leakage current density, a thicker film with high κ must be introduced to replace conventional $SiO_2$.

Based on previous research works, actually many studies have been done to replace $SiO_2$ layer as gate oxide such as $HfO_2$ [12–15], $ZrO_2$ [12,13,16–19], ZrON [19–24], $Al_2O_3$ [25–28], $TiO_2$ [1,9,12,16], $Ta_2O_5$ [1,9,12,16], and $Y_2O_3$ [29–35]. Unfortunately, each of them has their own limitations and drawbacks compared to $SiO_2$ layers. For $HfO_2$ and $ZrO_2$, six problems have been summarized in Chin et al. review paper [36]. There are (1) interfacial layer formation and growth during deposition and postdeposition annealing, (2) growth of microcrystal after heat treatment, (3) lateral oxidation at the gate edge, (4) existence of fixed charges, which causes flatband voltage shift, (5) higher interface states density, and (6) contamination of the dielectric from the precursors of chemical vapour deposited dielectric [36–39]. Large fixed charge and interface trap density are obtained in $Al_2O_3$ [40,41]. $TiO_2$ and $Ta_2O_5$ have too low conduction band offsets with Si conduction band and thermodynamic stability [42–44]. $TiO_2$ and $Y_2O_3$ are reported to have low crystallization temperature (< 400 °C) [45], which is unflavored in most of the processing temperatures of present MOS fabrication technology. Besides that, the interface density of $Y_2O_3$ ($10^{12}$ $eV^{-1}$ $cm^{-2}$) is too high for MOS device applications [46].

In this paper, the first section begins by discussing the lanthanide rare earth oxide (REO) as alternative gate oxide. After that, the common deposition methods included PVD and CVD were discussed. Following that, the deposition methods of each lanthanide REO and their performances as gate oxide were reviewed and enumerated. The next section pays particular attention to the literatures of the $Sm_2O_3$. Then, the previous deposition methods of the $Sm_2O_3$ as gate oxide were reviewed and compared. Lastly, the challenges to be overcome in the future are also reported in this review.

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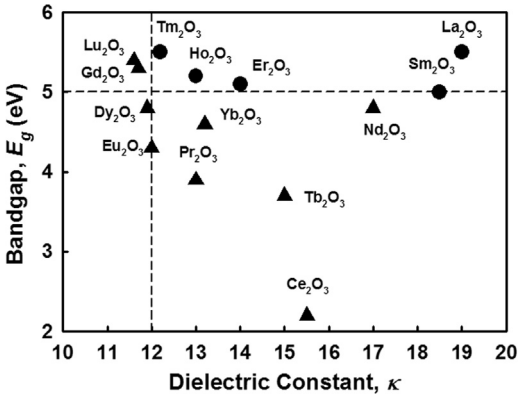


**Fig. 1.** The interrelationship between dielectric constant and bandgap of lanthanide REOs [36]. The black dots represented those oxides with higher dielectric constant ( > 12) and larger bandgap ( ≥ 5 eV).

## 2. Lanthanide rare earth oxide (REO) as alternative gate oxide

Recently, the lanthanide rare earth oxides (REOs) (Fig. 1) have been investigated due to some superior properties such as high dielectric constant, relatively large bandgap, high breakdown electric field, high resistivity, high conduction offset, low interface trap density, smooth surface, small lattice mismatch with silicon, and high thermal and chemical stability. REOs have been widely used in electronic devices such as, frequencies switches, reprogrammable memory circuits, capacitors, transistors, and varicaps [47–59]. The deposition methods, thickness, and electrical performances of lanthanide REOs films were summarized in Table 1.

The lanthanide REOs have higher dielectric constant (κ = between 7 and 30) than $SiO_2$ (κ = 3.9). High dielectric constant allows reducing equivalent oxide thickness (*EOT*) for downscaling purposes [54,60]. Higher dielectric constant can avoid using ultrathin thickness of gate oxides which may lead to undesirable current leakage due to direct tunneling of electron through gate oxides [61]. A high enough bandgap is also required for insulating properties. Normally, the bandgap should be higher than 5 eV. Only five of these lanthanide REOs are higher than 5 eV which is prior consideration as replacement candidate as shown in Fig. 2 [36].

REOs are predicted to be chemically or thermodynamically stable when in contact with Si substrates because they able to resist silicide formation after depositions. The oxygen tends to dissociate easily in air or oxygen during post deposition annealing. This will form $SiO_x$ interfacial layers or rare earth silicates layers. Undesirable interfacial layers may degrade the electric properties due to a reduced κ value. Thus, optimization of deposition parameters of gate oxides is required to minimize formation of interfacial layers [36,54,55,62,63].

Another concern of REOs is the hygroscopic property [62,63]. Hydride, $Ln_2O_3$-$H_2O$ will be formed after moisture absorption which may lead to form hydroxide, $Ln(OH)_3$. Undesirable hydroxide may increase film thickness and reduce the dielectric constant value. The hygroscopic property may roughen the surface of gate dielectric and increase leakage current density. The moisture reactivity of REOs is increasing as lattice energy, ionic radius and cations electronegativity of REOs are decreasing. Thus, $La_2O_3$ is the most hygroscopic (lowest electronegativity and highest lattice energy) while $Lu_2O_3$ is the least hygroscopic (highest electronegativity and lowest lattice energy) as shown in Fig. 3 [36,53,61,62].

## 3. Common deposition methods of lanthanide rare earth oxide (REO)

Many deposition methods (Table 1) have been developed for REOs thin films but they can be divided into two main and broad categories. The first one is chemical vapour deposition (CVD) such as metal organic-CVD (MOCVD), and atomic layer deposition (ALD), while second one is physical vapour deposition (PVD) such as sputtering (radio frequency (RF) and direct current (DC)), vacuum evaporation, thermal evaporation, electron beam evaporation, and pulsed laser deposition (PLD) [9,12,36,64,65].

### 3.1. Chemical vapour deposition (CVD)

The MOCVD applies basic principles of both CVD and ALD processes. The main difference between them is that MOCVD uses a metalorganic compound as precursor during deposition process [12]. A liquid precursor is advantageous to avoid or limit particle formations [9]. ALD is also known as atomic layer chemical vapour deposition (ALCVD) or atomic layer epitaxy (ALE) [12]. ALD is a thin film deposition process which involved the chemical gas phases and two precursors are deposited and oxidized alternatively in a sequential manner at substrates, called surface controlled growth cycles. The first precursor is introduced in excess and a monolayer of reactant is chemisorbed onto the surface. Then, the first precursor is removed by inert gas before the second precursor is introduced. The second precursor is reacted with the reactant on the surface and produce the desired film. Lastly, the second precursor is removed by inert gas again and the process is completed [36,65,66]. The precursor must be volatile, high purity, nontoxic, no gas phase reactions, no self-decomposition, and no etching of the existing oxide [2,65]. Good film quality, electrical properties, and low contaminations of films can be produced by thermal and plasma enhanced ALD [67]. Both MOCVD and ALD able to control the film thickness precisely with good uniformity and conformal coverage over complex shapes owing to the self-limiting growth mechanism of the precursors [2,9,12,36,65,66].

The chemical deposition methods are more widely used because of the advantages as mentioned in section before such as large area depositions, uniform film, good composition control, high film density, and deposition rates [9,47,64,65]. However, there still have some concerns in chemical depositions such molecular precursor availability, precursor stability, and volatility. High deposition temperatures and/or post deposition annealing are required to decompose metal organic precursors. Thus, large amounts of carbon may present which are detrimental to the electrical properties of the films [2,9,64,68]. As Wong and Chong summarized [12], ALD process has three main limitations: (1) too fine size of particles are difficult to transport from source to the film, (2) poor nucleation on hydrogen terminated silicon, and (3) residue contaminations. A typical example is the carbon content was left in $Nd_2O_3$ film which deposited by ALD process [68].

### 3.2. Physical vapour deposition (PVD)

For physical depositions, PLD requires a large energy density of laser beam to ablate the target source and vapourized the materials that eventually sublimate on the substrates [12]. PLD is a clean and simple method to obtain a wide range of structures, compositions, and properties [51]. In electron beam evaporation, an electron beam is used as power source to heat the target source to produce vapourized materials that condensed on substrates in high vacuum ambient [12]. Electron beam evaporation can produce ultrathin and smooth films with excellent electrical properties [12,48,69]. Dense and compact films with low stress can be deposited by electron beam evaporations [70]. The substrates suffer little damage since the electron beam sputters on the target source but not the substrates. However, it is not suitable as a conventional production method.

Sputtering is a process which source materials are ejected from the target source and deposited on the substrate in vacuum chamber [12,36]. DC and RF sputtering are the most common types of sputtering process. DC sputtering is used for target materials with good electrical conductivity while RF sputtering is used for target materials with low

**Table 1**
The thickness and electrical performances ($J$ = leakage current density; $E$ = electrical breakdown field; $C$ = capacitance; $D_{it}$ = interface trap density; $V_{FB}$ = flatband voltage; $EOT$ = equivalent oxide thickness; $E_g$ = bandgap; $Q_{ox}$ = oxide charge; $V_{th}$ = threshold voltage; $E_{trap}$ = trap energy; $CET$ = capacitance equivalent thickness; $N_t$ = trap density; $I$ = leakage current; $n$ = refractive index; $V_{BD}$ = breakdown voltage) of lanthanide REOs films which deposited by various methods.

| | Deposition method | Thickness (nm) | $\kappa$ | $J$ (A cm$^{-2}$) | $E$ (MV cm$^{-1}$) | $C$ | $D_{it}$ (cm$^{-2}$ eV$^{-1}$) | Others | Remarks | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|
| La | Electron beam evaporation | ~ 2 | – | – | – | ~ 1.3 μF cm$^{-2}$ | ~ $10^{11}$ | $V_{FB}$ = 0.5 V<br>$EOT$ = 0.5 nm | LaSiO | [78] |
| | | 1.7 – 2.2 | – | – | – | ~ 4 μF cm$^{-2}$ | – | $EOT$ = 0.37 – 0.48 nm | | [75] |
| | | ~ | – | ~ $10^{-7}$ | – | – | – | $V_{FB}$ = −0.9 V | Al-doped | [76] |
| | | 4 | – | ~ $10^{-1}$ | – | – | – | $V_{BD}$ = 2.8 V<br>$V_{th}$ = 0.067 V | $CeO_x/La_2O_3$ | [81] |
| | | 10 | – | ~ $10^{-7}$ | – | – | – | $E_{trap}$ = 0.19 eV | | [69] |
| | | 4 | – | – | – | ~ 0.8 μF cm$^{-2}$ | – | $V_{FB}$ = 0.65 V | $HfO_x/La_2O_3$ | [212] |
| | | ~ | – | 6.67 × $10^{-7}$ | – | ~ 1.5 μF cm$^{-2}$ | – | $EOT$ = 2.33 nm | | [73] |
| | MOCVD | ~ 40 | ~ 23.5 | – | – | ~ 800 ρF | – | $EOT$ = 1.8 nm<br>$E_g$ = 6.18 eV<br>$V_{FB}$ = 0.7 V | | [74] |
| | | 25–105 | – | – | – | ~ 0.1 μF cm$^{-2}$ | 1.5 × $10^{11}$ | $V_{FB}$ = −0.7 V<br>$Q_{ox}$ = 3 × $10^{11}$ cm$^{-2}$ | | [77] |
| | PE-ALD | 4 | – | 8 × $10^{-7}$ | – | ~ 2.5 μF cm$^{-2}$ | ~ 2 × $10^{11}$ | $Q_{ox}$ = 2.8 × $10^{11}$ cm$^{-2}$ | | [67] |
| | PLD | 2 | – | – | – | – | – | – | $La_2Hf_2O_7$ | [82] |
| Ce | Electron beam evaporation | 3 | – | – | – | – | – | – | | [84] |
| | | 3 | – | – | – | – | – | $E_g$ = 7.67 eV | | [85] |
| | | 1 | – | ~ $10^{-4}$ | 1 | – | – | – | $CeO_2/La_2O_3$ | [87] |
| | | 110–500 | 90 | 0.1 × $10^3$ | – | ~ 1.4 nF | – | $n$ = 2.5<br>$V_g$ = + 1 V | | [86] |
| | First Principle Calculation | – | 24.3 | – | – | – | – | – | | [83] |
| | PLD | 135–350 | – | – | – | – | – | – | | [91] |
| | MOCVD | 33 | – | – | – | – | – | – | $La_xCe_yO_z$ | [92] |
| | RF sputtering | 50 | – | – | – | – | – | – | $CeO_2/SiO_2$ | [90] |
| | | 12 | – | – | – | ~ 100 pF | – | – | | [89] |
| Pr | CVD | ~ 100 | – | – | – | – | – | – | | [93] |
| | Laser ablating | 110 | – | – | – | – | – | – | | [100] |
| | Thermal evaporation | 0.7 | – | – | – | – | – | – | | [101] |
| | MOCVD | 7–32 | 8–15 | – | – | 0.35 μF cm$^{-2}$ | 3 × $10^{11}$ | $CET$ = 7–16 nm | | [98] |
| | | 9 | – | – | – | – | – | – | | [99] |
| | | 15 | 16–24 | ~ $10^{-7}$ | – | – | 2 × $10^{12}$ | $N_t$ = 1.6 × $10^{11}$ cm$^{-2}$<br>$Q_{ox}$ = 4.77 × $10^{11}$ cm$^{-2}$ | | [95] |
| | MBE | 3 – 8.1 | – | – | – | – | – | – | | [102] |
| | | 6 | – | – | – | – | – | – | | [107] |
| | | 5.5 | 12 | ~ $10^{-7}$ | – | – | – | $V_{FB}$ = - 1.3 eV | $Pr_xSi_yO_z$ | [97] |
| | | 7–10 | – | – | – | – | – | – | | [103] |
| | Electron beam evaporation | 0.202 | – | – | – | – | – | – | | [104] |
| | | 18 | – | – | – | – | – | – | | [105] |
| | | 13.4 | – | – | – | – | – | – | | [106] |
| | | 18 | 30 | ~ $10^{-10}$ | 43 | 4500 ρF | | $V_g$ = 6 V<br>$E_g$ = 3.2 eV<br>$EOT$ = 1.4 nm | | [96] |
| | Ion beam synthesis | 450 | | – | – | – | – | – | | [108] |
| Nd | RF Sputtering | 27 | – | ~ $10^{-5}$ | ~ 7 | – | – | $EOT$ = 89 Å | | [109] |
| | | 25 | – | ~ $10^{-5}$ | ~ 11 | – | – | – | | [110] |
| | Thermal evaporation | 172.2 | 10.2 | – | – | – | ~ 3.3 × $10^{18}$ | $N_t$ = ~ 2 × $10^{23}$ m$^{-3}$ | | [111] |
| | ALD | ~ 250 | 10.5 | 3.2 × $10^{-9}$ | 1.3 | – | – | $V_{FB}$ = −0.2 V | | [68] |
| Sm | RF Sputtering | 7.5–8.2 | 14.3 | ~ $10^{-7}$ | – | ~ 1.3 μF cm$^{-2}$ | ~ 1 × $10^{12}$ | CET = 2.76–5.79 nm | | [48] |
| | | 25 | – | ~ $10^{-3}$ | 15 | – | – | – | | [184] |
| | | 120 | – | ~ $10^{-5}$ | – | 7.65 nF | – | $\Delta N_{ot}$ = −2.5 × $10^{10}$ cm$^{-2}$<br>$\Delta N_{it}$ = 2.5 × $10^{11}$ cm$^{-2}$ | | [185] |
| | | 61 | – | ~ $10^{-6}$ | – | – | – | – | | [182] |
| | | 118 | – | – | – | 4.78 nF | – | – | | [57] |
| | DC Sputtering | 120 | 10.4 | ~ $10^{-7}$ | – | – | – | – | | [183] |
| | MOCVD | 120 | – | – | – | – | – | – | | [47] |
| | Thermal evaporation | 122.2 | 42.7 | – | – | – | – | $E_g$ = 4.33 eV | | [49] |
| | Vacuum evaporation | 230–300 | | – | – | ~ 115 pF | – | $E_g$ = 2.92 eV<br>$N_{ss}$ = 3.4 × $10^{10}$ cm$^{-2}$ eV$^{-1}$ | | [50] |
| | Resistive evaporation | ~ | 13 | – | 7 | ~ 0.05 μF cm$^{-2}$ | – | $N_{ss}$ = 7 × $10^{11}$ cm$^{-2}$ eV$^{-1}$ | | [52] |
| | PLD | 61.4 | – | ~ $10^{-8}$ | 0.2 | – | – | – | | [51] |
| | ALD | 50 | 10 | 1.1 × $10^{-8}$ | 0.38 | 0.364 pF | – | $V_{FB}$ = −0.2 V | | [56] |
| Eu | Sol-gel | – | – | – | – | – | – | $N_t$ = ~ 9.98 × $10^{12}$ cm$^{-2}$<br>$V_{th}$ = 3.28 V<br>$\mu_{FE}$ = 2.8 × $10^{15}$ cm$^{-3}$ | Eu-In-Zn | [113] |
| | Thermal evaporation | 185.8 | ~ 29.4 | – | – | – | – | Wm = 3.9 eV<br>$N_{LS}$ = ~ 2.1 × $10^{24}$ cm$^{-3}$ | | [114–116] |

(continued on next page)

**Table 1** *(continued)*

| | Deposition method | Thickness (nm) | $\kappa$ | $J$ (A cm$^{-2}$) | $E$ (MV cm$^{-1}$) | $C$ | $D_{it}$ (cm$^{-2}$ eV$^{-1}$) | Others | Remarks | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | $V_{FB}$ = −0.48 V<br>$Q_{ox}$ = - 3.67 × 10$^{11}$ cm$^{-2}$<br>$N_t$ = ~ 3.99 × 10$^{12}$ cm$^{-2}$ | | |
| | MOCVD | 50–500 | 12 | – | – | 1100 ρF | – | $N_f$ = ~ 6 × 10$^{10}$ cm$^{-2}$ | | [112] |
| Gd | Reactive sputtering | ~ 6 | – | ~ 10$^{-4}$ | ~ 5 | ~ 1.4 fF μm$^{-2}$ | ~ 2 × 10$^{11}$ | – | | [124] |
| | | ~ 200 | 7.4 | ~ 10$^{-7}$ | – | ~ 3.2 fF μm$^{-2}$ | ~ 4 × 10$^{10}$ | $EOT$ = 10 nm | | [72] |
| | Modified Epitaxy Process | 5.9 | – | ~ 10$^{-9}$ | – | 1.4 nF | – | – | | [117] |
| | PLD | 10 | 6 | ~ 10$^{-1}$ | – | ~ 550 nF cm$^{-2}$ | – | $Q_{ox}$ = - 8 × 10$^{11}$ cm$^{-2}$<br>$EOT$ = 7 nm | | [125] |
| | | 500 | – | – | – | – | – | $E_g$ = 5.8 eV | | [120] |
| | LPCVD | 35 | 14.67 | ~ 10$^{-6}$ | ~ 8 | – | – | $EOT$ = 7.13 nm | | [118] |
| | PE-CVD | 12 | 15.6 | 4 × 10$^{-6}$ | – | – | ~ 1.8 × 10$^{11}$ | $EOT$ = 3 nm | | [213] |
| | CVD | 19 | 21 | ~ 10$^{-3}$ | 4.0 | – | – | – | $Gd_xSc_yO_z$ | [214] |
| | RF sputtering | 8 | – | – | – | ~ 170 pF | – | – | | [119] |
| | | 30 | 17.2 | ~ 10$^{-6}$ | – | ~ 280 pF | – | – | | [126] |
| | | 6 | ~ 29 | ~ 10$^{-8}$ | 3.0 | – | – | $E_g$ = 6.19 eV | | [215] |
| | Anodic oxidation | 12 | 12.2 | ~ 10$^{-7}$ | – | ~ 109 pF | – | $EOT$ = ~ 3.7 nm | | [121] |
| | EB-PVD | 1360 | 20 | – | – | – | – | – | | [122] |
| | Dual ion beam deposition | 25.5 | 20 | – | – | 4.1 × 10$^{-7}$ F cm$^{-2}$ | – | $V_{FB}$ = 9.0 V | | [130] |
| | Sol gel | 729 | – | – | – | – | – | – | | [131] |
| | Electron beam evaporation | 2 | – | – | – | – | – | – | | [132] |
| | PE-ALD | 10 | – | – | – | – | – | – | | [134] |
| | ALD | 10 | – | ~ 10$^{-8}$ | 15 | ~ 0.6 μF cm$^{-2}$ | ~ 10$^{11}$ | $EOT$ = ~ 5 nm | | [216] |
| | Thermal evaporation | 130.8 | 7.47 | – | – | – | – | $V_{FB}$ = - 1.12 V | Gd-In-O | [128,129] |
| | | 187.2 | 7.5 | – | – | – | – | $N_t$ = ~ 10$^{28}$ m$^{-3}$ | | [217] |
| | | 5–20 | 11.4 | – | – | ~ 0.8 μF cm$^{-2}$ | – | $EOT$ = ~ 4 nm | | [127] |
| | MBE | 5.9 | 11 | 3 × 10$^{-8}$ | – | 2 nF | ~ 10$^{12}$ | $CET$ = 2.2 nm<br>$Q_{ox}$ = 3 × 10$^{12}$ cm$^{-2}$ | | [218] |
| Tb | RF Sputtering | 25 | – | – | – | – | – | $I$ = ~ 10$^{-4}$ A<br>$V_{BD}$ = −15 V | | [135] |
| Dy | Reactive sputtering | 10 | 10.41 | 9.18 × 10$^{-8}$ | – | ~ 0.9 μF cm$^{-2}$ | ~ 1.3 × 10$^{11}$ | – | | [137] |
| | | ~ 10 | 19.3 | ~ 10$^{-8}$ | – | ~ 1.7 μF cm$^{-2}$ | ~ 7 × 10$^{11}$ | $CET$ = 2.02 nm | $Dy_2TiO_5$ | [139] |
| | | 5–12 | – | ~ 3 × 10$^{-3}$ | – | – | – | $EOT$ = 2.3 nm | | [138] |
| | Thermal evaporation | 165 | 9.2 | – | – | – | 8.3 × 10$^{15}$ | $V_{FB}$ = 0.14 V<br>$Q_{ox}$ = - 3.6 × 10$^{15}$ m$^{-2}$ | | [136] |
| | | 140 | 5.2 | – | – | – | 1.85 × 10$^{9}$ | $V_{FB}$ = - 1.26 V<br>$Q_{ox}$ = 0.74 × 10$^{15}$ m$^{-2}$ | Dy-Mn | [140,141] |
| | | 342 | – | – | – | – | – | $E_g$ = 5.8 eV | | [142] |
| | ALD | 10 | – | – | – | – | – | – | $HfDyO_x$ | [144] |
| | | 0.5–0.8 | – | – | – | – | – | – | ZrDyO | [219] |
| | MOCVD | 20 | 22 | ~ 10$^{-5}$ | 2.3 | ~ 0.8 μF cm$^{-2}$ | – | $CET$ = ~ 4 nm | $DyScO_3$ | [143] |
| | Electron beam evaporation | ~ 80 | 18 | – | – | ~ 0.26 μF cm$^{-2}$ | – | $I$ = 1.85 × 10$^{-8}$ A | | [220] |
| Ho | RF Sputtering | ~ 30 | – | – | – | – | – | – | | [147] |
| | | 11 | ~ 10.1 | ~ 10$^{-9}$ | – | 0.8 μF cm$^{-2}$ | ~ 3 × 10$^{11}$ | – | | [145] |
| | Sol-gel | – | – | – | – | – | – | – | Mn-doped | [146] |
| | ALD | 7.7–27.5 | – | ~ 10$^{-9}$ | – | ~ 22 nF mm$^{-2}$ | – | – | Ti-doped | [148] |
| | | 7.7–49 | – | – | – | – | – | – | Ti-doped | [221] |
| Er | ALD | 15 | 11.8 | ~ 10$^{-8}$ | | | | $V_{FB}$ = 0.3 V | | [149] |
| | | 10–100 | – | – | – | – | – | – | | [150] |
| | Laser Ablation | 30 | – | – | – | – | – | – | | [154] |
| | Cathodic Arc deposition | 100–200 | – | – | – | – | – | – | | [151] |
| | Thermal evaporation | ~ 196 | 12.1 | – | – | – | 1.3 × 10$^{12}$ | $V_{FB}$ = - 0.2 V<br>$Q_{ox}$ = - 2.6 × 10$^{11}$ cm$^{-2}$ | | [155] |
| | | 210 | 12.42 | – | – | ~ 510 μF m$^{-2}$ | 7.94 × 10$^{11}$ | $Q_{ox}$ = - 1.77 × 10$^{11}$ cm$^{-2}$<br>$\Delta V_{FB}$ = 0.55 V | Er-Mn | [157] |
| | | ~ 196 | – | – | – | – | – | $E_g$ = 0.07 eV<br>$N_t$ = 2.4 × 10$^{25}$ m$^{-3}$ | | [156] |
| | Reactive sputtering | ~ 12 | – | – | – | – | – | – | | [160] |
| | | ~ 40 | – | – | – | ~ 325 nF cm$^{-2}$ | – | $V_{TH}$ = 0.36 V | $Er_xTi_yO_z$ | [153] |
| | | 45 | – | – | – | ~ 0.65 nF | 1.3 × 10$^{11}$ | $EOT$ = 4.5 nm<br>$V_{FB}$ = - 0.05 V | Er silicate | [163] |
| | RF sputtering | 35 | 10.19 | ~ 10$^{-7}$ | ~ 7 | ~ 56 pF | – | $EOT$ = 15.3 nm | | [152] |
| | | 80 | – | – | – | – | – | $E_g$ = 6.17 eV | | [161] |
| | | 80 | – | – | – | – | – | $E_g$ = > 4.5 eV | | [159] |
| | Electron beam evaporation | 125–200 | – | – | – | – | – | $E_g$ = 5.72 eV | | [164] |
| | Ion beam sputtering | 0.5–2 | – | – | – | – | – | $E_B$ = 0.665 eV | Ni/Er/Si | [162] |

*(continued on next page)*

**Table 1** *(continued)*

| | Deposition method | Thickness (nm) | κ | $J$ (A cm$^{-2}$) | $E$ (MV cm$^{-1}$) | $C$ | $D_{it}$ (cm$^{-2}$ eV$^{-1}$) | Others | Remarks | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|
| Tm | MBE | 0.67–4 | 10.8 | $2 \times 10^{-3}$ | 1 | – | – | $EOT$ = 2.3 nm | | [171] |
| | Reactive sputtering | 12 | – | $\sim 10^{-8}$ | – | 1.1 μF cm$^{-2}$ | $\sim 10^{12}$ | $CET$ = 31.1 Å | | [166] |
| | | ~ 15 | ~ 28.1 | $10^{-8}$ | – | 1.8 μF cm$^{-2}$ | 7.32 × $10^{11}$ | $CET$ = 1.98 nm | $Tm_2Ti_2O_7$ | [168] |
| | MBE | ~ 5 | – | – | – | – | – | $E_g$ = 5.76 eV | | [165] |
| | ALD | ~ 2 | – | $10^{-5}$ | – | 1.0 μF cm$^{-2}$ | $2 \times 10^{11}$ | $EOT$ = 0.1–0.3 nm | TmSiO | [172] |
| | | ~ | ~ 5.1 | – | – | 2.0 μF cm$^{-2}$ | $\sim 10^{10}$ | $EOT$ = 1.6 nm<br>$V_{FB}$ = 0.1 V | TmSiO/HfO | [169] |
| Yb | Electron beam evaporation | 1.1 | 46.2 | – | – | 3.27 μF cm$^{-2}$ | ~ 2.4 × $10^{11}$ | $EOT$ = 0.79 nm<br>$V_{FB}$ = −4.6 V<br>$Q_{ox}$ = 2.8 × $10^{11}$ cm$^{-2}$ | | [173] |
| | Reactive sputtering | ~ 8 | 11.4 | 1.81 μ | – | 1.29 μF cm$^{-2}$ | – | $V_{FB}$ = −0.78 V | | [174] |
| | Thermal evaporation | 300 | 7.1 | – | – | – | – | $E_g$ = 4.32 eV | Yb-Mn | [170] |
| | RF Sputtering | 20 | – | – | – | – | – | $I$ = ~ $10^{-8}$ A<br>$V_{BD}$ = ~ 1 V | | [222] |
| Lu | PLD | 4.5 | – | ~ 2.6 × $10^{-5}$ | – | ~ 1000 ρF | – | $EOT$ = 1.1 nm | | [177] |
| | Reactive sputtering | ~ 6 | 12.8 | – | – | ~ 55 ρF | – | $V_{FB}$ = −2.93 V<br>$N_t$ = 4.87 × $10^{18}$ cm$^{-3}$ | | [178] |
| | MBE | 6 | – | – | – | – | – | $N_t$ = 2 × $10^{17}$ cm$^{-3}$ eV$^{-1}$<br>$V_{th}$ = 0.5 V | $LaLuO_3$ | [223] |
| | | 5 | – | ~ $10^{-7}$ | – | ~ 198 ρF | – | $CET$ = 18.6 Å | $LaLuO_3$ | [180] |
| | | 10 | – | – | – | ~ 1.5 μF cm$^{-2}$ | – | $EOT$ = 1.9 nm | $LaLuO_3$ | [224] |
| | | 20–40 | – | – | – | – | – | $E_g$ = 5.4 eV | | [225] |
| | ALD | 6.3 | ~ 30 | ~ $10^{-10}$ | – | ~ 1.1 μF cm$^{-2}$ | – | $CET$ = 3.1 nm | $LaLuO_3$ | [181] |
| | | 0.8–9 | – | – | – | – | – | – | | [226] |
| | First Principle | – | ~ 19 | – | – | – | – | – | | [227] |
| | Calculation | – | – | – | – | – | – | $E_g$ = 5.8 eV | | [228] |

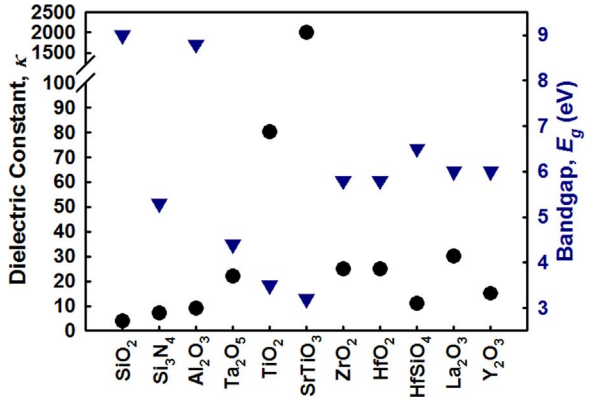


**Fig. 2.** Dielectric constant and bandgap values of common high κ oxides [2,42,211].

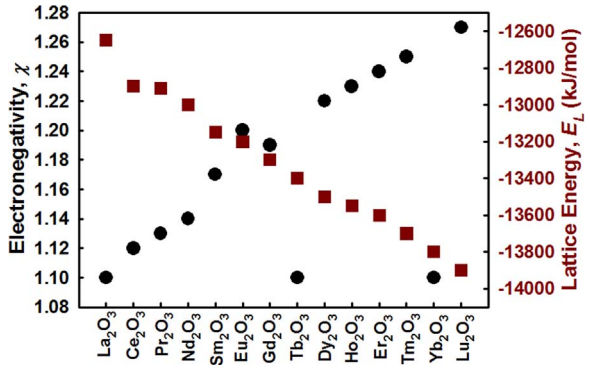


**Fig. 3.** The electronegativity and lattice energy of lanthanide REOs [36,53].

electrical conductivity [12]. For RF magnetron sputtering, a magnet is involved to increase the concentration of electron ionizations and lengths of electron paths thus increase the ionization efficiency [36]. Sputtering has a high deposition rate, low substrate temperatures rise, good adhesion between films and substrates, and is broadly available [2,71]. Even though straightforward sputtering of metal or metal oxide target is easier than other methods but it may oxidize the Si substrate and form a thick $SiO_2$ interlayer or metal silicate layer during deposition process [16,72]. Besides that, sputtering only deposits in line of sight so it do not give good coverage on complex shape [2].

## 4. Deposition methods of lanthanide REO films and their performances

### 4.1. Lanthanum (La) oxide

Since lanthanum oxide ($La_2O_3$) has high κ (~ 27) and large interface barrier with Si substrates, it was seen as a suitable replacement for conventional $SiO_2$ layer as gate oxide [67,69,73–77]. Based on previous works, $La_2O_3$ films were deposited by e-beam evaporation [69,73,76,78], MOCVD [74,77], molecular beam epitaxy (MBE) [75], and ALD [67].

The formation of La-silicates at the $La_2O_3$ films and Si substrates interface and fairly good metal–oxide–semiconductor field-effect transistor (MOSFET) operations were observed [78]. Kawanago et al. [78] conducted 3 steps of annealing (annealing in oxygen ambient, forming gas annealing (FGA) at 800 °C, and 420 °C) after $La_2O_3$ films deposition by e-beam evaporation to solve the oxygen defects without degrading the interfacial properties. The binding energy was increased without increasing the La-silicate thickness [78]. For $La_2O_3$ films by e-beam evaporation followed by post deposition annealing (PDA), film thicknesses were decreased before PDA at 300 °C due to film densification while film thickness were increased after PDA at 300 °C owing to growth of an interfacial silicate layer. A lower leakage current (6.67 × $10^{-7}$ A cm$^{-2}$) was observed if annealed at higher temperatures [73]. In Sen et al. [69] works, the trapping characteristics of $La_2O_3$ films deposited by e-beam evaporations were improved after annealing at 600 °C due to removal of O vacancies and the formation of $SiO_2$ layers.

For CVD at a deposition temperature of 600 °C at low pressure, smooth amorphous features were detected and the RMS increased after PDA in oxygen ambient. A flatband voltage of 1.3 V and dielectric constant of 23.5 were reported in Cheng et al. works [74]. The $La_2O_3$

thin films deposited at 250 °C by e-beam evaporation were smoother than films deposited at room temperature. The leakage current density at 1.0 V was $1.7 \times 10^{-8}$ A cm$^{-2}$ with 1.26 of *EOT* [13]. In Yang et al. works, smooth $La_2O_3$ films deposited by e-beam evaporation remained amorphous up to 900 °C. The amorphous films have a smaller roughness and larger bandgap. With the increase of annealing time, the fixed charge density was increased significantly. The dielectric constant and leakage current density were determined to be 15.5 and $7.56 \times 10^{-6}$ A cm$^{-2}$, respectively [70]. The transconductances and drain current can be improved by scaling down the *EOT* which can suppress the formation of La-silicate layers [75]. Relative low average interface trap density ($2 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$) and leakage current density ($8 \times 10^{-7}$ A cm$^{-2}$) can be obtained by pulse-enhanced pulsed laser deposition (PE-PLD) deposition [67].

For $La_2O_3$ films deposited by MOCVD, the dielectric constants, flatband voltages, and oxide charges density were improved after annealing in oxygen ambient. The flatband voltages and oxide charges density were further improved while the dielectric constant remained the same if FGA [77]. In Wong et al. [76] works, Al ions were introduced into $La_2O_3$ films by plasma immersion ion implantation. The flatband voltages of the samples annealed at 400 °C shift to more negative side because implanted Al ions were not fully activated and interstitial atoms served as positives charges. The flatband voltages were reduce to −0.9 V after RTA at 600 °C with post metallization annealing (PMA) [76].

For the $La_2O_3$ doped $SiO_2$ (LSO) films deposited by e-beam evaporation remained amorphous up to 800 °C. An interfacial layer of $SiO_2$ layer was formed due to diffusion of oxygen towards the Si substrate [79]. Compared to single $La_2O_3$ gate stack, $La_2O_3/Y_2O_3$ double gate stack able to reduce the $SiO_2$ and silicate layer formation [80]. For $CeO_x/La_2O_3$ gate stacks, oxygen vacancies in the $La_2O_3$ films can be filled with oxygen from $CeO_x$ due to reduction of $CeO_x$ [81]. La was also doped in Hf oxide which remained amorphous at higher temperature, had lower defect densities and lower lattice mismatch with Si than others REOs [82]. For $CeO_x$ and $La_2O_3$ stacking gate oxides, the $Ce^{3+}$ ions were reduced from $Ce^{4+}$ ions releasing the oxygen which diffused into $La_2O_3$ films. $Ce_xO_y$ is able to store or release oxygen and reduce the defects during $La_2O_3$ formation because of its good oxygen storage capacity. The $CeO_x/La_2O_3$ stacks of transistors have larger transconductance, smaller subthreshold slope and better hot carrier robustness compared to single $La_2O_3$ stack of transistor [81].

### 4.2. Cerium (Ce) oxide

Cerium dioxide or ceria ($CeO_2$) has been widely used in catalytic applications and also in Si-based optoelectronics. $CeO_2$ is highly absorbing in the UV region and is optically transparent in the visible spectral regions [2] However, its lattice spacing may expand by 0.6 due to oxygen defect formations in oxygen poor conditions [3]. Trivalent $Ce^{3+}$ at grain boundaries and around O vacancies occurred as defective regions in amorphous $Ce_2O_3$ films. The $CeO_2$ ($Ce^{4+}$) may reduce to $Ce_2O_3$ ($Ce^{3+}$) and the bandgap will reduce from around 6 eV to around 2 eV [83]. In previous studies, $CeO_2$ films were deposited by e-beam evaporation [81,84–88], ion beam assisted deposition (IBAD) [85], reactive sputtering [89,90], and PLD [91].

In $CeO_2$ films grown by reactive evaporation, Ce silicates were formed between $CeO_2$ and the both Si (111) and (100) substrates after annealing. Disappearance of $Ce^{4+}$ in XPS peaks may be due to formation of cerium silicates or $Ce_2O_3$ phases [84]. In Logothetidis et al. [86] works, the $CeO_2$ films were deposited by e-beam evaporation and IBAD. IBAD produced films exhibited much larger grains compared to e-beam evaporation produced films. Amorphous interface layers were formed in all cases. However, interfaces of IBAD produced samples were rougher due to ions bombardment during deposition [86]. For $CeO_2$ films deposited by sputtering followed by RTA, the intensity of XRD peaks and surface roughness were increased as the annealing temperatures increased owing to film crystallization. The $CeO_2$ films annealed at 950 °C exhibit the largest memory window of 4.7 V [89]. For $CeO_2/SiO_2$ films deposited by sputtering followed by RTA, the samples annealed at 800 °C have strongest crystallization, largest grain size, and highest root mean square (RMS) value.

Balakrishnan et al. [91] proposed deposition of $CeO_2$ films by PLD. The crystallite sizes and surface roughness were increased as the substrate temperatures increased. The $CeO_2$ films deposited at 973 K exhibited better epitaxial nature than those deposited at lower temperatures [91]. Mamatrishat et al. reported that Ce silicate layers were formed after annealing. The energy bandgap and valence band offset of Ce silicate with respect to silicon were determined to be at 7.67 eV and 4.35 eV, respectively. The concentration of $Ce^{3+}$ ions decreased and that of $Ce^{4+}$ ions increased at interface between $CeO_2$ films and Si substrates [85].

Since 2012, $CeO_2$ films have been used as capping layer on $La_2O_3$ as gate dielectric layer [81,87,88]. The high oxygen vacancies of $La_2O_3$ films can be overcome by deposition of $CeO_2$ films on the top. The $CeO_2$ films can be self-adapted and supply extra oxygen atoms to $La_2O_3$ films [88]. The electrical performance was improved compared to single $La_2O_3$ films [81,87,88]. In Lim et al. [92] works, $La_xCe_yO_z$ films were deposited by metal organic decomposition. The microstrains of $La_xCe_yO_z$ films reduced while the crystallite sizes increased when both annealing temperatures and time were increased. Si nanocrystal was found in the $SiO_x$ interface layer owing to thermal decomposition of $SiO_x$ at high temperature annealing process [92].

### 4.3. Praseodymium (Pr) oxide

Praseodymium oxide, $Pr_2O_3$ was widely used in photocatalytic materials, anodes of LEDs, CMOS, and DRAM technologies [93–97]. Previously, $Pr_2O_3$ films were deposited by MOCVD [93–95,98,99], PLD [100], thermal evaporation [101], MBE [97,102,103], e-beam evaporation [96,104–107], and ion beam synthesis [108].

Amorphous $PrO_x$ films were observed at low partial oxygen pressure of MOCVD process. $Pr_6O_{11}$ films tend to form at higher partial oxygen pressures (40–100 Pa) and lower growth temperatures while $Pr_2O_3$ films tend to form at lower partial oxygen pressures (0.027–0.6 Pa) and higher growth temperatures [93]. Hexagonal $Pr_2O_3$ crystals of smaller grain size were formed in dominantly amorphous $PrO_2$ films at higher oxygen partial pressure of MOCVD. Cubic $Pr_2O_3$ and Pr silicates were formed after PDA in $N_2$ atmosphere while hexagonal $Pr_2O_3$ and Pr silicate were formed after PDA in vacuum atmospheres [98]. The $Pr_2O_3$ films were crystallized at 800 °C in oxygen ambient but remain amorphous in argon ambient. However, the silicate layers were formed at 900 °C in argon ambient. No Pr silicide was found in both ambients [99].

Polycrystalline $Pr_2O_3$ films were deposited by MOCVD and multi interface layers ($Pr_2O_3$/Pr silicate/$SiO_2$/Si) were found. The dielectric constant, flatband voltage, and leakage current density of the $Pr_2O_3$/Pr silicate/Si stack were determined to be 26, 0.4 V, and $5 \times 10^{-10}$ A cm$^{-2}$, respectively [94]. The Pr oxide films were amorphous if MOCVD deposition temperatures were lower than 600 °C. The thickness of Pr silicate layers was increased with the deposition temperature. The leakage current density and breakdown electrical fields for 15 nm polycrystalline $Pr_2O$ films were $1 \times 10^{-7}$ A cm$^{-2}$ and 4.5 MV cm$^{-1}$, respectively. A dielectric constant of 16 and flatband voltage of 0.1 V were reported [95]. In Mane et al. [97] works, the $Pr_xSi_yO_z$ films were deposited by MBE. The dielectric constant, flatband voltage shift, and leakage current density were determined to be 12, −1.3 eV, and $10^{-7}$ A cm$^{-2}$, respectively [97]. Si was added during growth of $Pr_2O_3$ by MBE. The added Si enhanced the nucleation at initial stages and restricted the atomic intermixing by forming the silicate interlayer. Hexagonal $Pr_2O_3$ was more stable at higher temperature than cubic $Pr_2O_3$ and restricted the oxygen diffusion through the layer due to its higher density. However, the overall leakage current density still quite

high (~ $10^{-1}$ A $cm^{-2}$) as a gate oxide [102].

$PrSi_2$ films were formed in the as-deposited films under oxygen deficient atmosphere during MBE. $Pr_2O_3$ films disappeared for samples annealed at 900 °C. However, the silicidation of Pr can be suppressed by supplying additional oxygen gas [103]. $PrO_2$ phases were preferred to grow at initial stages due to lower lattice mismatch. $SiO_2$ layers may act as stress buffer during transformation of $PrO_2$ to $Pr_2O_3$ [104]. The $Pr_2O_3$ films grown epitaxially on Si (001) by MBE displayed high κ (~ 30), low leakage current (~ $10^{-4}$ A $cm^{-2}$), and high breakdown voltage field (43 MV $cm^{-1}$). The structural quality of epitaxially grown films degraded after being exposed to air due to oxygen diffused through $Pr_2O_3$ and formation of $SiO_x$ layer. However, this can be suppressed by aluminum capping on $Pr_2O_3$ films [96,105–107]. For $Pr_2O_3$ films deposited by ion beam synthesis, Pr silicide was detected at lower annealing temperatures while Pr silicates were detected at higher annealing temperatures [108].

### 4.4. Neodymium (Nd) oxide

Neodymium oxide ($Nd_2O_3$) was selected for electronic applications not only for its high dielectric constant value but also for its good step coverage and good dielectric strength [109,110]. According to previous studies, $Nd_2O_3$ films were deposited by reactive RF sputtering [109,110], thermal evaporation [111], and ALD process [68].

Strong $Nd_2O_3$ film structures were formed on polycrystalline Si substrates by reactive RF sputtering after rapid thermal annealing (RTA) at 900 °C [109,110]. The binding energies shifted to higher energies compared to as-deposited film. The RMS of as-deposited films improved from 5.61 nm to 4.81 nm after RTA at 900 °C. $Nd_2O_3$ structures exhibited strongest intensities for (002)-, (102)-, and (110)-oriented structures. The annealed samples at 900 °C have the highest electrical breakdown field (~ 6 MV $cm^{-1}$) and lowest gate voltage shift (~ 0.1 V) among the annealed samples [109,110].

Anne Kosola et al. [68] reported that $Nd_2O_3$ films deposited by ALD were crystallized at higher annealing temperatures. Residual contaminants such as carbonates from precursors were detected in Fourier transform infra-red (FTIR) spectra. The RMS of annealed samples (1.0 nm) had increased compared to as deposited samples (0.8 nm). The flatband voltages shifted to positive bias from −2.5 V to −2.2 V when alternating current (AC) frequencies increased from 100 kHz to 500 kHz. About 10.5 of dielectric constant of annealed samples were obtained by calculation. The leakage current of $Nd_2O_3$ films was very low, around 3.2 × $10^{-9}$ A $cm^{-2}$ and the breakdown field strength was around 1.3 MV $cm^{-1}$ [111].

### 4.5. Europium (Eu) oxide

Europium oxide ($Eu_2O_3$) was used in optoelectronics, microelectronics, and laser applications. In Singh et al. works, the thin $Eu_2O_3$ films were deposited by low pressure MOCVD methods. The dielectric constant of $Eu_2O_3$ films grown at 600 °C was about 12. The flatband voltages decreased when the deposition temperatures increased owing to removal of Eu deficient parasitic phases and better crystallinity of the films [112].

Based on previous works, europium (Eu) has been widely used as doping element in indium oxide or indium-zinc oxide (IZO) by sol-gel spin coating technique [113] or thermal evaporation to form MOS structures [114–116]. Eu acted as carrier suppressor in IZO due to its low electronegativity (1.2) and standard electrode potential (−1.991 V). Furthermore, $Eu^{3+}$ ions (0.095 nm) have similar ionic radius and same charges with $In^{3+}$ ions (0.08 nm). Thus, extra free charge carriers were not produced if $In^{3+}$ ions were replaced by $Eu^{3+}$ ions. Lower RMS roughness of EIZO samples (1.01 nm) were observed when compared to un-doped samples (1.88 nm) [113]. For thermally evaporated Eu-In oxide films followed by RTA at 800 °C in vacuum, dielectric constants as high as 29.4 and barrier heights of 3.9 eV were reported in Dakhel's works [114–116].

### 4.6. Gadolinium (Gd) oxide

Gadolinium oxide, $Gd_2O_3$ has many applications in electronics, photonics, and nuclear industries [72,117–123]. Based on previous researches, $Gd_2O_3$ films were deposited by sputtering followed by plasma oxidation [124], modified epitaxy process [117], PLD [120,125], sputtering [72,119,123,126], low pressure-CVD [118], thermal evaporation [127–129], anodic oxidation [121], electron beam-PVD [122], dual ion beam deposition [130], sol-gel method [131], e-beam evaporation [132,133], and ALD [134].

Amorphous $Gd_2O_3$ films of 6 nm thickness can be achieved by plasma oxidation. However, $SiO_x$ and $GdO_x$ layers formed between Si substrates and $Gd_2O_3$ films. The dielectric constants of $Gd_2O_3$ films were about 14. The interface state density and leakage current density were improved after annealing [124]. At RTA temperatures of 930 °C after modified epitaxy process, the Gd were fully replaced or resolved by the TiN gates. No $Gd_2O_3$ films were shown and only thicker interfacial layers were shown in HRTEM. The on/off current ratios and leakage current density were ~ $10^6$ and ~ $10^{12}$ A $cm^{-2}$, respectively [117].

For PLD methods, Mishra et al. [120] reported that the amorphous $Gd_2O_3$ films were formed at lower substrate temperatures and only monoclinic $Gd_2O_3$ films were observed when substrate temperatures were above 673 K. The surfaces roughness was mainly affected by substrate temperature with no significant effects by various oxygen partial pressures [120]. $Gd_2O_3$ and TiN seed layers were deposited by PLD methods. TiN seed layers were able to prevent oxidation of Si substrates and diffusion between Gd and Si substrates. Existence of Gd $(OH)_3$ due to the hygroscopic characteristics of REOs. High leakage currents occurred due to O vacancies at grain boundaries. Hence, a relatively low dielectric constant (~ 6) and high leakage current density (0.1 A $cm^{-2}$) were observed [125].

Hexagonal Gd films were formed at RTA between 100 °C and 250 °C after high pressure sputtering but disappeared at higher temperatures. Monoclinic $Gd_2O_3$ formed below 350 °C while cubic $Gd_2O_3$ were observed at 500 °C and above. However, hexagonal $GdSi_2$ was observed too. The leakage current densities improved when oxidation temperatures and FGA temperatures increased. The interface state density of samples FGA at 450 °C (4 × $10^{10}$ $eV^{-1}$ $cm^{-2}$) were lower compared to samples FGA at 300 °C (1.7 × $10^{12}$ $eV^{-1}$ $cm^{-2}$) [72]. The preferred orientation of (401)-structures deposited by LP-CVD possessed strong and well crystallizations which is suitable for sensing applications. The dielectric constants improved from 11.14 to 14.67 after as-deposited films were annealed at 900 °C. A relatively high breakdown field of ~ 7 MV $cm^{-1}$ was observed [118].

For $Gd_2O_3$ films deposited by RF sputtering, the surface roughness increased with increase in RTA temperatures. The electrical performances and overall storage capability improved after RTA [119]. Cubic phase of $Gd_2O_3$ films were observed at lower growth temperatures and monoclinic phases of $Gd_2O_3$ films dominated at higher growth temperatures of RF sputtering deposition. The cubic phase of $Gd_2O_3$ films exhibited better electrical properties than the monoclinic phases of $Gd_2O_3$ films [126]. Gadolinium silicates with a thickness of 1.7 nm were observed at the interface layers between $Gd_2O_3$ films and Si substrates after thermal evaporation deposition of $Gd_2O_3$ films. The dielectric constant of $Gd_2O_3$ films was determined to be 11.4 [127].

For anodic oxidation, the film structures were not affected by magnitude of bias voltages instead by the oxidation times. Gd-silicate layers did not form but $SiO_2$ interfacial layers were observed. For anodization voltages of 30 V, the electrical performance improved with the increase of anodization times while the electrical performance improved with decrease of anodization times for 60 V. The $Gd_2O_3$ films dissipated and disappeared for samples anodized at 60 V and 40 min [121].

For EB-PVD methods, cubic phase was observed at higher deposition temperatures and higher oxygen flow rates. However, monoclinic phase was observed for samples with thicker films. The grain size increased with the increase of film thickness and deposition temperatures. The dielectric constants increased with the decrease of oxygen flow rates. Samples with relatively low deposition temperatures (200 °C) and oxygen flow rates (25 and 50 sccm) had the highest dielectric constants of 20 [122]. Monoclinic structures with smaller grain sizes appeared at lower substrate temperatures for dual ion beam epitaxy deposition methods. Oxygen deficiencies prevented the ratio of Gd and O from achieving 3:2. High flatband voltages of 9.0 V indicated high charge density in the oxide owing to oxygen deficiencies [130]. Crystallization started at an annealing temperature of 400 °C after sol gel deposition and the grain size increased with annealing temperature [131].

Zr incorporated $Gd_2O_3$ films deposited by e-beam evaporation have better crystalline structure by impeding the growth of Gd-silicate interfacial layers and reducing oxygen activation barriers. However, the Zr atoms may cause lattice constant shrinkage as the Zr radius is smaller than the Gd radius [132]. Amorphous of GdN films with low concentration of impurities and good uniformity were deposited at lower temperatures by ALD [134]. Smooth and uniform stoichiometric orthorhombic $GdTiO_3$ films were deposited by reactive sputtering method. The dielectric constants and threshold voltages of $GdTiO_3$ films were determined to be ~ 15 and 0.14 V respectively. A high $I_{on}/I_{off}$ ratio of $4.2 \times 10^8$ was observed due to high electron mobility (32.3 $cm^2 V^{-1} s^{-1}$) and low leakage currents (~ $10^{-12}$) [123].

No interfacial layers were formed between as-deposited Gd silicate films and Si substrates after deposition by e-beam evaporation. However, a $SiO_2$ interfacial layer was formed after annealing in oxygen ambient [133]. For Gd-In oxide films deposited by thermal evaporation, the Gd oxides crystallized alone and the grain growth of $In_2O_3$ was enhanced in an atmosphere with higher oxygen concentration. The dielectric constants decreased from 7.47 to 4.46 due to the formation of silicate layers when the annealing temperatures increased from 400 °C to 600 °C [128,129].

### 4.7. Terbium (Tb) oxide

Terbium oxide ($Tb_2O_3$) has been widely used in MOSFET device application such as optical glasses and colour TV tubes. In Kao et al. [135] works, the $Tb_2O_3$ films were formed on strained Si:C substrates by reactive RF sputtering followed by RTA. The crystallinity (higher intensity), binding energy (from 149 eV to 528.7 eV), RMS of surface (from 5.67 nm to 4.07 nm), RMS of interface (from 5.85 nm to 1.7 nm), gate voltage shift (from −2.0 V to −0.5 V), leakage current (from $10^{-4}$ A $cm^{-2}$ to $10^{-5}$ A $cm^{-2}$), and electrical breakdown voltage (from −6 V to −14 V) of annealed samples were improved compared to as-deposited films [135].

### 4.8. Dysprosium (Dy) oxide

The ionic radius of Dysprosium oxide, $Dy_2O_3$ is relatively larger than Si which means it reacts poorly with Si substrates and no or little formation of silicate layers [136]. These superior properties attracted many researchers to study and investigate its suitability as gate oxide material. Based on previous literatures, $Dy_2O_3$ films were deposited by reactive sputtering [137–139], thermal evaporation [136,140–142], MOCVD [143], and ALD [144].

Preferred orientation of (100)-planes of cubic dysprosium and (400)-planes of $Dy_2O_3$ were formed by reactive sputtering. The surface roughness increased with increase of RTA temperatures. However, silicon atoms from the substrate and oxygen from $Dy_2O_3$ moved to interface regions and formed a low κ interfacial layer during RTA at 800 °C. Thus, amorphous silica layers were formed, leading to smaller surface roughness. The samples annealed at 700 °C had a better dielectric constant (10.41), lower leakage current density (9.81 nA $cm^{-2}$), and smaller interface state density ($1.26 \times 10^{12}$ $eV^{-1}$ $cm^{-2}$) [137].

Fine grained and amorphous films can be achieved by lower deposition rate of reactive evaporation. Smooth Dy silicate interfaces were confirmed by good agreement between measured and stimulated *C-V* curves which indicated a low density of interface traps. For oxygen annealing, there is a more uniform distribution of crystallization compared to argon annealing [138]. Dakhel [136] reported that [111]-orientation grains decreased by increasing PDA temperatures and in vacuum environment compared to atmosphere annealing after thermal evaporation of $Dy_2O_3$ films. In Al-Kuhaili et al. [142] works, the $Dy_2O_3$ films were deposited by thermal evaporation followed by PDA at various temperatures (200–800 °C). The Dy hydroxide and Dy hydroxide carbonates were converted to $Dy_2O_3$ after PDA at 800 °C. The $Dy_2O_3$ films annealed at 600 °C exhibited the smoothest surface and the best optical properties [142].

$DyMnO_3$ started to crystallize at temperatures higher than 600 °C after thermal evaporation which was better and higher than the crystallization temperatures of the $Dy_2O_3$ (300 °C) and $Mn_2O_3$ (500 °C). $DyMnO_3$ grains with [200]-orientation were grown with increasing annealing temperatures. Samples annealed at 1000 °C in air atmosphere have a lower interface state density ($1.85 \times 10^{15}$ $eV^{-1}$ $m^{-2}$) and higher dielectric constants (5.2) [140,141]. Titanium adding of $Dy_2TiO_5$ by RF sputtering was able to suppress the hydroxide thickness. $SiO_2$ layers were almost unaltered at high temperature (≤ 800 °C). However, oxygen atoms were moving from $Dy_2TiO_5$ to the interfacial layer to form silicate and $SiO_2$ at RTA temperatures of 900 °C. The surface roughness increased with the increase of RTA temperatures. The $Dy_2TiO_5$ annealed at 800 °C exhibited thinner *CET* of 2.02 nm, smaller interface state density of $7 \times 10^{11}$ $eV^{-1}$ $m^{-2}$, and lower hysteresis voltage of about 10 mV [139]. Hardy et al. [144] reported that a $HfO_2$ layer can act as a barrier layer to prevent Dy-silicate formation during ALD process. He also reported that Dy may prevent the monoclinic $HfO_2$ crystallization in $HfDyO_x$ [144]. For $DyScO_3$ films deposited by MOCVD, the dielectric constant and breakdown field were determined to be 22 and 2.3 MV $cm^{-1}$, respectively [143].

### 4.9. Holmium (Ho) oxide

Holmium oxide ($Ho_2O_3$) was attracted to be used in optoelectronics, logic devices, memory devices, and pH sensing films. $Ho_2O_3$ possess the highest lattice energy, largest magnetic moment and susceptibility among the REO and can easily be crystallized prior to annealing process [145,146]. According to previous literatures, Ho $_2O_3$ films have been deposited by reactive RF sputtering [145,147], sol-gel method [146], and ALD [148].

In Pan et al. [145,147] works, poorly crystalline of $Ho_2O_3$ films were formed by reactive sputtering before RTA process. The crystallinity and binding energy improved after RTA process. However, the crystallinity decreased when the RTA reached at 900 °C due to the formation of amorphous silica layers at the interface between $Ho_2O_3$ films and Si substrates. This trend was supported by the binding energy of Ho-O bonds decreasing suddenly but Si–O bonds increasing for samples annealed at 900 °C. The surface roughness increased when RTA temperatures increased, but the RMS was decreased at 900 °C. This may be due to holmium and oxygen atoms migrating to interface layers and forming amorphous silica layers with lower surface roughness at higher RTA temperature (900 °C) [145,147].

For Mn-doped $Ho_2O_3$ films deposited by sol-gel methods, the crystallite sizes decreased with the Mn contents but the strains increased with the Mn contents [146]. In Castan et al. works, the $HoTiO_x$ films were grown by ALD process. The higher Ho content of $HoTiO_x$ films have lower capacitance values but less leaky which have lower leakage current density [148].

### 4.10. Erbium (Er) oxide

Erbium oxide, $Er_2O_3$, is also an attractive candidate material for gate oxide because it has small ionic radius and appropriate electronegativity which suppress the hydroxylation [149–153]. According to previous literatures, $Er_2O_3$ films have been deposited by ALD [149,150], laser ablation [154], cathodic arc deposition [151], thermal evaporation [155–158], LP-CVD [152], reactive sputtering [71,159–163], and e-beam evaporation [164].

In Xu et al. [149] and Paivasaari et al. [150] works, polycrystalline $Er_2O_3$ films were deposited by ALD method. The grain sizes and surface roughness increased with increasing of annealing temperature. Er-silicates were formed at 1000 °C due to inter-diffusion between $Er_2O_3$ films and $SiO_2$ interfacial layers. The dielectric constant increased from 9.8 to 11.8 while the flatband voltages decreased from 0.66 V to 0.3 V after annealing at 600 °C. The hysteresis voltage decreased significantly indicating that the trapped charges density was reduced efficiently. The leakage currents were increased after annealing due to the presence of grain boundaries which acted as leakage paths compared to amorphous as-deposited films [149]. Amorphous films can be obtained at low deposition temperatures and the $SiO_2$ layer hinders the heteroepitaxial $Er_2O_3$ film [150]. Smoother and highly textured surfaces can be deposited by laser ablation methods compared to electron beam evaporation techniques [154].

In Adelhelm et al. [151] works, the monoclinic B-phase $Er_2O_3$ films with dense structures were deposited by filtered cathodic arc deposition resulting in ion bombardment irradiation damage and high internal stress during particle formation. The $Er_2O_3$ films deposited by thermal evaporation followed by PDA in vacuum conditions suffered more structural oxygen vacancies compared to PDA in dry oxygen atmospheres. The samples annealed in vacuum exhibited better electrical results which have a lower interface state density ($1.3 \times 10^{12}$ $eV^{-1}$ $cm^{-2}$) and higher dielectric constant (~ 12.1) compared to samples annealed in dry oxygen atmospheres [155,156]. An Er-silicate interface layer was formed after reactive sputtering deposition followed by RTA at 800 °C resulting in an increase of surface roughness due to migration of Er atoms to the interfacial layer and the formation of an amorphous silicate layer [160].

However, Kao et al. reported that RTA at 800 °C after low pressure CVD had smoother surface roughness than samples before RTA due to increasing grain size and crystallization. The dielectric constant of annealed $Er_2O_3$ films with *EOT* of 153 Å was 10.19. The reported leakage current density and breakdown electrical field of annealed at 800 °C samples were ~ $10^{-7}$ A $cm^{-2}$ and ~ 7 MV $cm^{-1}$ [152]. In Wu et al. [71] works, the effects of substrates temperatures during RF magnetron sputtering were investigated. The compressive stress becomes larger when the substrate temperatures increased from room temperature to 200 °C [71]. The amorphous and stoichiometric $Er_2O_3$ films can be formed by RF sputtering of an $Er_2O_3$ target in Ar ambient [159,161]. Sub-stoichiometric $Er_2O_3$ films can be achieved by e-beam evaporation with a substrate temperature of 300 °C without oxygen atmosphere [164].

The doped $Er_2O_3$ films or Er-doped films have attracted great attention owing to their potential applications in MOS and integrated optics. During thermal evaporation deposition, $Mn_2O_3$ and $Er_2O_3$ do not crystallize seprately but $ErMnO_3$ compounds were preferable to form as reported in Dakhel's works [157]. Stable crystalline solid solutions of Er-Gd oxides were detected in samples which were PDA in oxygen and vacuum atmospheres after thermal evaporation depositions [158].

For reactive co-sputtering of Er and Ti, amorphous of $ErTi_xO_y$ films remained even after annealing process. The surface roughness increased with the PDA temperature. The dielectric constant, field effect mobility, and threshold voltage of $Er_2TiO_5$ annealed at 400 °C were determined to be 14.6, 8.24 $cm^2$ $V^{-1}$ $s^{-1}$, and 0.37 V, respectively [153]. Er interlayer was found to increase the NiSi formation temperatures of ion beam sputtering process. However, Er interlayers did not significantly improve the Schottky barrier heights of the Ni/Er/Si system [162]. Er-silicate films were formed in $Er/SiO_2/Si$ stacking systems after RTA process. The oxygen atoms which were supplied by $SiO_2$ were diffused to Si substrates and formed the Er-silicate layers during RTA [163].

### 4.11. Thulium (Tm) oxide

Thulium oxide ($Tm_2O_3$) is also one of the potential replacements of $SiO_2$ [165–170]. Based on previous literatures, $Tm_2O_3$ films were deposited by reactive sputtering [166,168], MBE [165,167,171], and ALD [169,172].

Single crystalline $Tm_2O_3$ films can be achieved by atomic oxygen assisted MBE growth followed by ultra-high vacuum annealing at 800 °C. The dielectric constant (~ 10.8) and leakage current density (~ $2 \times 10^{-3}$ A $cm^{-2}$) improved after annealing process. A higher oxygen partial pressure may degrade the crystallinity due to the formation of thick $SiO_x$ interface layers which cannot be removed by in-situ ultra-high vacuum (UHV) annealing. Thus, large orientation distributions of mosaic structures were formed [165,167,171]. The bandgap of $Tm_2O_3$ was determined to be 5.76 eV [165].

Preferred (400)-oriented was formed by reactive sputtering by RTA at 800 °C in oxygen ambient. According to the X-ray photoelectron spectroscopy (XPS) spectra, the energy of $SiO_2$ layers increased and energy of $Tm_2O_3$ films decreased for samples underwent RTA at 800 °C. The surface roughness increased with RTA temperature due to crystallization during annealing. The samples annealed at 700 °C have a lower leakage current density compared to 800 °C due to leakage paths along the grain boundaries [166,168]. TmSiO films with 2 nm thickness can be formed without presence of $SiO_x$ by ALD following by PDA at 750 °C in nitrogen ambient. The silicate layer thickness increased with the PDA temperature. The capacitance density, *EOT*, and interface state density of TmSiO films improved after PDA process [172].

### 4.12. Ytterbium (Yb) oxide

Ytterbium oxide ($Yb_2O_3$) forms high quality interfaces with Si substrates with low interface trap density ($2.4 \times 10^{11}$ $cm^{-2}$ $eV^{-1}$), and low fixed oxide charge density ($2.8 \times 10^{11}$ $cm^{-2}$) [173]. The most preferable (222)-oriented of $Yb_2O_3$ were obtained by RTA at 800 °C after reactive sputtering. However, intensity of $SiO_2$ layers increased at higher RTA temperature (800 °C) due to maintain the Yb-silicate structures by the $SiO_2$ interface layers [174].

According to previous researches, Yb was also used as dopant for transition metal oxides. The Yb dopants were able to stabilize the cubic phase and improve leakage current in $HfO_2$ [175]. Yb also had low solid solubility and formed well grain boundaries in $In_2O_3$ film [176]. Chen et al. [175] reported that Yb may led to crystallographic change from monoclinic to cubic phase of $HfO_2$. Monoclinic $HfO_2$ was stable at room temperature but cubic only existed at high temperature environment due to oxygen vacancies presence by compensated Yb charge states. The dielectric constant increased from 16.1 to 28.4 compared to undoped $HfO_2$ [175]. Dakhel [170] reported that in the presence of $Yb_2O_3$, $Mn_2O_3$ did not crystallize because Mn ions diffused into the inter-grain boundaries either in amorphous $Yb_2O_3$ structures or crystalline $Yb_2O_3$ structures. At high concentrations of Yb-doped $In_2O_3$, non-crystalline structures were formed with larger lattice parameter due to the larger ionic radius of $Yb^{3+}$ than $In^{3+}$. The dielectric constants reached about 81.6 for 8.5 wt% Yb-doped $In_2O_3$ [176].

### 4.13. Lutetium (Lu) oxide

Lutetium oxide ($Lu_2O_3$) was predicted to show good insulating properties, thermal stability, hygroscopic immunity, and lower leakage current [177–179]. Previously, $Lu_2O_3$ films were deposited by reactive sputtering [178] and PLD [177,179].

Amorphous $Lu_2O_3$ films can be achieved by PLD followed by PDA at

600 °C in nitrogen ambient. The leakage current density at 1 V was 2.6 × $10^{-5}$ A $cm^{-2}$ with an *EOT* of 1.1 nm [177]. RTA at 900 °C after reactive sputtering may cause Lu-silicate formation. This was shown by the higher intensity of Lu-silicate peaks in XPS and lower intensity of $Lu_2O_3$ in X-ray diffraction (XRD) peak compared to RTA at 800 °C. The dielectric constants (from 9.1 to 12.8) and breakdown voltage fields (from 3.4 MV $cm^{-1}$ to 3.53 MV $cm^{-1}$) were improved by RTA process. The samples annealed at 800 °C exhibited the highest flatband voltage shift of about 2.93 V [178]. For $Lu_2O_3$ films deposited by PLD, Lu-silicate was formed after PDA process. However, the lattice strains were decreasing when the PDA temperatures increased [179].

Combinations of superior properties of both La (high crystallization temperatures and high dielectric constant) and Lu (low hygroscopic and reactivity) were investigated by forming $LaLuO_3$ film [180]. $LaLuO_3$ has high κ (~30) and is thermally stable up to 1000 °C. $LaLuO_3$ deposited by MBE still remain amorphous after RTA at 700 °C and 900 °C. However, a $LaLuO_3$-silicate interfacial layer was formed and increased in thickness with RTA temperatures. The leakage current density was increased after annealing at 900 °C [180]. For the $LaLuO_3$ deposited by ALD, as-deposited films were smooth and remained amorphous up to 1000 °C. The dielectric constants was improved from 17 to 30 after annealing process [181].

## 5. Samarium oxide, $Sm_2O_3$ as alternative gate oxide

$Sm_2O_3$ is one of the promising candidate materials among rare earth oxides because of some outstanding properties such as high κ (7–22), high breakdown electric field (5–7 MV $cm^{-1}$), relatively large bandgap (4.33 eV), low leakage current, large conduction offset with Si, high thermal stability, small frequency dispersion, low trapping rate, and low hygroscopic characteristic [36,47–50,52,57,58,182–185].

Among the relatively high bandgap (> 5 eV) lanthanide REOs, $Sm_2O_3$ has the lowest flatband voltage (0.1 V) and lowest leakage current (1.1 × $10^{-8}$ A $cm^{-2}$) [36,56]. Even though the $Ho_2O_3$ has low leakage current density (1.2 × $10^{-8}$ A $cm^{-2}$) but its high flatband voltage (6.9 V) is not preferred [36,56]. Besides that, some researchers have shown that $Sm_2O_3$ films have a lower leakage current density (2.5 × $10^{-6}$ A $cm^{-2}$) than $La_2O_3$ (0.9 × $10^{-4}$ A $cm^{-2}$) [36,66,186].

Among the lanthanide REOs, $Sm_2O_3$ has the second highest κ value and has a relatively large bandgap as shown in Fig. 2 [36,48,57,182,183,185]. $Sm_2O_3$ is also predicted to be thermodynamically stable on Si substrates [48,57,183–186]. Moreover, $Sm_2O_3$ is less hygroscopic than $La_2O_3$ because it has a smaller ionic radius and is less electropositive as shown in Fig. 3 [36,57].

In previous works [47,48], Shalini and Shivashankar reported that $Sm_2O_3$ films deposited by MOCVD were strongly oriented due to the small lattice mismatch (0.6%) between cubic $Sm_2O_3$ and Si substrates. Rozhkov et al. reported that a relatively high barrier energy (2.72 eV) and breakdown field (5–7 MV $cm^{-1}$) were obtained at Si- $Sm_2O_3$ interfaces [50,52]. Constantinescu et al. [51] measured dielectric constants ranging from 14 to 16 in the capacitance measurements. A relatively low threshold voltage (0.79 V) and large mobility (6.25 $cm^2$ V $cm^{-1}$ s) were reported in Chen et al. work owing to the smooth interface is formed between the $Sm_2O_3$ and indium-gallium-zinc oxide (IGZO) layer [183]. A dielectric constant as high as 20 was obtained from calculations by Kaya et al. [185]. The resistivity of $Sm_2O_3$ films deposited under various sputtering power and temperatures varied from 1.1 × $10^8$ $\Omega^{-1}$ $cm^{-1}$ to 2.5 × $10^6$ $\Omega^{-1}$ $cm^{-1}$ [57].

## 6. Deposition methods used for $Sm_2O_3$ films

According to previous works, the $Sm_2O_3$ films have been deposited by both PVD and CVD methods as summarized in Table 2. Fig. 4 shows the summary of leakage current density – electrical breakdown field (*J-E*) characteristic of $Sm_2O_3$ films deposited by various previous methods. Sputtering was the most common deposition method. The $Sm_2O_3$ films were deposited by direct sputtering of $Sm_2O_3$ target or pure samarium target followed by post deposition annealing or oxidation. Some researchers deposited the $Sm_2O_3$ films by RF magnetron sputtering with $Sm_2O_3$ and or Sm targets [48,57,182,184,185] while only one researcher deposited the $Sm_2O_3$ films by DC magnetron sputtering with Sm target [183]. In Kaya et al. works [57], effects of sputtering power and substrate temperature on composition and structural quality of $Sm_2O_3$ films were proven. The smoothest and best crystallinity of $Sm_2O_3$ films were formed at 200 W sputtering power and a substrate temperature of 200 $^0$C.

**Table 2**
Summary of thickness, surface roughness, and interfacial layer characterization methods of $Sm_2O_3$ films deposited by various previous methods.

| Deposition methods | Thickness (nm) | RMS (nm) | Interfacial layer characterization methods | Ref. |
|---|---|---|---|---|
| ALD | 50 | 1.2 | – | [56] |
| DC sputtering | 120 | 3.43–7.81 | XPS | [183] |
| MOCVD | 120 | 3.9–7.9 | – | [47] |
| PLD | 61.4 | 5–10 | SEM | [51] |
| Thermal evaporation | 122.2 | – | – | [49] |
| Vacuum evaporation | 230–300 | – | – | [50] |
| RF sputtering | 61 | – | TEM | [182] |
| | 120 | – | – | [185] |
| | 110–125 | 5.2–19.5 | – | [57] |
| | 25 | – | XPS | [184] |
| | 7.5–8.2 | 0.19–0.37 | XPS | [48] |

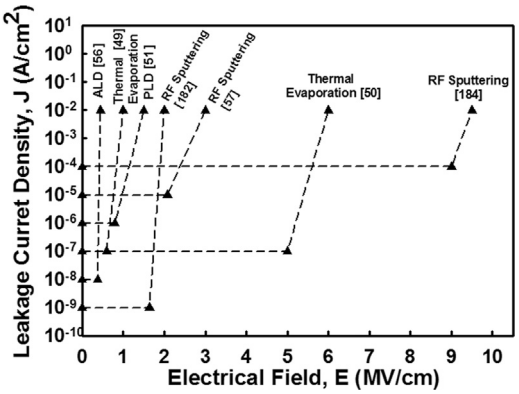


**Fig. 4.** Summary of leakage current density – electrical breakdown field (*J-E*) characteristic of $Sm_2O_3$ films deposited by various previous methods.

In Pan et al. work [48], they concluded that RF magnetron sputtering was able to produce thin film (7 nm) with lower leakage current ($10^{-7}$ A $cm^{-2}$ at 1 V). Recently, some researchers proved that PDA after RF magnetron sputtering can improve structural and electrical properties such as increase capacitance density, and reduce surface roughness and leakage current [186,187]. In another study by Pan et al., they reported that PDA can improve the electrical properties of $Sm_2O_3$ thin film on Si substrates. The best improvement of sample which is PDA at 700 °C which gives the highest dielectric constant and the lowest leakage current density while reducing the *EOT* values [186].

Vacuum and thermal evaporation are another physical route of deposition methods [49,50,52]. In Rozhkov et al. works [50,52], $Sm_2O_3$ was evaporated onto Si substrates after thermal oxidation of samarium in air. The samarium was oxidized in air before evaporated on Si substrates. An effective dielectric constant as high as 42.7 was calculated from the Schottky current formula in Dakhel's work [49]. The $Sm_2O_3$ films can also be deposited by RF-PLD which produced good quality and amorphous $Sm_2O_3$ films [51]. The laser ablation was involved in PLD where target material evaporated when irradiated by an intense laser beam and deposited on the substrate.

Besides that, highly crystalline $Sm_2O_3$ films with low lattice mismatch had been grown by MOCVD using phenanthroline adducts of pentadionate complexes [47]. In MOCVD, decompositions of metal organic precursors were involved and transported by carrier gas before being deposited on substrate after certain surface chemical reaction occurred. The $Sm_2O_3$ films were also grown by ALD. The films produced by ALD had good electrical properties such as high dielectric constant (~ 29) and relatively high bandgap (5 eV) [187]. In Paivasaari et al. work [56], the 0.38 MV $cm^{-1}$ of breakdown field and 1.1 × $10^{-8}$ A $cm^{-2}$ were reported for the $Sm_2O_3$ films deposited by ALD.

## 7. Future challenges

Silicon dioxide is the traditional gate oxide on the silicon substrate since few decades ago. Limited thickness scaling ability due to performance restrictions has led to development of new replacement materials especially the high dielectric constant materials. Unfortunately, the surface and/or interface quality became another issue when new materials deposited on the silicon substrates. In this issue, there are some challenges that lie ahead researchers. The surface and/or interface quality is important since it will affect the electrical performances and lifetime of the devices. A good surface and/or interface should has good adhesion between oxide and substrate and no downgradable interlayer such as silicates, silicides, etc. Thus, many deposition methods are developed and proposed in order to produce best surface and/or interface quality. Many efforts have been done on conventional high dielectric constant materials such as Zr, La, Hf, etc. to improve the adhesion and reduce and/or control the growth of interlayers such introduction of nitrogen, annealing process, etc. However, there are more details are left to emerge the feasibility of lanthanide REOs as the gate oxide. Previous researchers reported that fairly good interface quality of lanthanide REOs with high dielectric constant can be produced since REOs has low lattice mismatch with silicon. Nevertheless, there are still lack of information regarding the surface and/or interface analysis and dielectric properties of lanthanide REOs. Hence, intensive study of interface quality and dielectric properties are required to fully discover the possibility of lanthanide REOs as a gate oxide. Meanwhile, exploration of deposition method as well as oxidation or nitration mechanisms are also paramount to produce a good surface and/or interface quality.

For ultrathin gate oxides, leakage current always dominated by direct tunneling which when applied gate voltage lower than barrier height [188–190]. The triangular potential barrier arises and Fowler-Nordheim (FN) tunneling dominates when high gate voltage is applied [188–190]. Conventional Wentzel-Kramers-Brillouin (WKB) approximation is used to calculate tunneling current by calculating transmission coefficient across potential barriers [190–193]. WKB approximation is applicable for devices with single dominant tunneling mechanism [192]. A parabolic dispersion which applicable for hole tunneling in oxide with thickness below 2 nm at low gate voltage (direct tunneling) is assumed in most of models instead of non-parabolic dispersion [194,195]. Besides that, Schrodinger-Poisson equation is also used to calculate tunneling current. Since this theoretical model does not include electron distribution in energy sub-bands, a self-consistent Schrodinger-Poisson equation introduced which interface trap charge and fixed oxide charge in oxide region are taken into account [196–198]. The interface trap charge and fixed oxide charge play important role when the tunneling current is weak [196].

Direct tunneling equations reveals that tunneling current is not only determine by dielectric constant ($\kappa$) only, but also effective tunneling mass ($m_{eff}$) and barrier height ($\Phi_B$) [189,193,199–201]. Large increase of κ value generally lead to decrease of $m_{eff}$ and $\Phi_B$. The $m_{eff}$ and $\Phi_B$ depend on the oxide thickness [193,195,201–204], oxidation temperature [202,205], and nitrogen concentration [204,206,207]. Typically, $m_{eff}$ is extracted from *I-V* measurement by fitting *I-V* measurement into analytic expressions. However, it is not applicable over a wide oxide thickness and bias range [195]. Many studies and researches have been done on calculation of $m_{eff}$ in different effective working condition regimes of leakage current mechanisms such as resonant tunneling [198,208], Fowler-Nordheim (FN) tunneling [192,202,205,209], and direct tunneling [194,195,199,210]. However, in most of cases, especially in FN tunneling calculation, the $m_{eff}$ always assumed by a number which extracted from previous references and then $\Phi_B$ is calculated [201,205]. In Ng et al. works [206], they determined $m_{eff}$ and $\Phi_B$ by fitting *I-V* measurement into direct tunneling (thin films) and FN tunneling (thick films) without assuming a value of either $m_{eff}$ and $\Phi_B$. A wide range of values of $m_{eff}$ for gate oxides may obtain by using different models and approximations.

To authors' knowledge, there are many studies on $m_{eff}$ of silicon dioxide and silicon oxynitride, but still limited works on rare earth oxides. There are only few works on $La_2O_3$ [199,203]. The effective tunneling mass is important parameter in MOS devices due to the device functionality is determined by its magnitude. Therefore, gate leakage current suppression should not focus on dielectric constant only, exploration on estimation or calculation of effective tunneling mass for rare earth oxides by different theoretical models or analytical expressions are also needed in the future.

## 8. Conclusion

A review of the development of REOs gate oxide was presented. $SiO_2$ gate oxide was widely utilized because of its excellent physical and chemical properties. However, its usages were limited by aggressive miniaturization of MOS devices. High leakage current and undesirable power dissipation may occurred in extreme thin gate oxide. Reliability issues limited the thickness scaling. Thus, new replacement of gate oxide material with physically thicker but same electrically *EOT* was needed. Some high dielectric constant materials such as $HfO_2$, $ZrO_2$, $Al_2O_3$, $La_2O_3$, $TiO_2$, $Ta_2O_5$, and $Y_2O_3$ were investigated. However, each of them has their own drawbacks compared to $SiO_2$. Deposition methods for REOs thin films can be divided into two categories: (1) PVD and (2) CVD. Last few decades, lanthanide REOs had been investigated because lanthanide REOs have high dielectric constant, relatively large bandgap, high breakdown electrical field, high conduction offset, low interface trap densities, small lattice mismatch with Si, and high both thermal and chemical stability. Numerous deposition methods included both CVD and PVD methods had been utilized to deposit and form the REOs thin films on Si substrates. Among lanthanide REOs group, samarium oxide was more preferred and discussed because of its relatively low flatband voltage, low leakage current, high dielectric constant, relatively high bandgap and high conduction offset values. Based on previous works, samarium oxides had been deposited by both CVD and PVD methods. Sputtering is one of the most common deposition methods for samarium oxide. A good surface and/or interface quality of gate oxide is required and important since it will affect the electrical performances and lifetime of the devices. This left some challenges to be overcome for researchers in the future.

## Competing interests

The authors declare that they have no competing interests.

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