Influence of applied voltage on the physical and electrical properties of anodic Sm_2O_3 thin films on Si in 0.01 M NaOH solution

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Formation of anodic samarium oxide thin film by anodisation of 15 nm thin sputtered samarium metal on silicon substrate was systematically investigated. Sputtered Sm on Si substrate was followed by anodisation in 0.01 M NaOH (pH 11) at various applied voltages (10, 15, 20, and 25 V). All anodisation processes were performed for 10 min at room temperature in the bath with constant stirring. The crystallinity of Sm_2O_3 film was evaluated by X-ray diffraction analysis. The crystallite size of Sm_2O_3 was calculated by Scherrer equation. The cross-section of 20 V sample was examined by high-resolution transmission electron microscope. The sample anodised at 20 V demonstrated the highest electrical breakdown field of 9.50 MV/cm at 10^{-4} A/cm^2. This is attributed to the lowest effective oxide charge, slow trap charge density, average interface trap density, and total interface trap density.

1. Introduction: International Technology Roadmaps of Semiconductors (ITRS) predicts that continued scaling of complementary metal–oxide–semiconductor devices requires thinner (<1 nm) and higher dielectric constant gate oxides than that of the commonly used SiO_2. Several oxides with higher dielectric constant or termed high-κ dielectric have been proposed as alternative to SiO_2. Wilk *et al.* [1] has reviewed on the possibility of the use of various binary oxides to be used as gate oxide. Other works reported on the use of TiO_2 [2, 3], Al_2O_3 [4], ZrO_2 [2, 4–7], ZrON [8–15], HfO_2 [4, 16], TaO_2 [1, 3, 4], and Gd_2O_3 [17], as high-κ gate oxide to replace SiO_2.

Of these oxides, Sm_2O_3 has been seen as one of the most promising candidates due to its high dielectric constant (~15), a wide bandgap (4.33 eV), high conduction barrier (>1 eV), high breakdown electric field (5–7 MV/cm), and its good thermal stability when in direct contact with Si [14, 18–25]. Various deposition methods have been studied, such as metallo-organic chemical vapour deposition [26], pulsed laser deposition (PLD) [27], thermal evaporation [28], vacuum evaporation [29], resistive evaporation [30], anodisation [25], direct current (DC), and radio frequency (RF) sputtering [14, 20, 21, 31, 32].

Anodisation is one of the electrochemical methods which is considered as an alternative deposition methods owing to its simplicity, cost efficiency, low thermal budget, less pinholes, and good uniformity of films [17, 33–35]. Moreover, anodisation do not need expensive equipment, clean furnace toxic chemical, and any special condition (e.g. high vacuum chamber) compare to others methods [36]. Anodisation has been widely used to grow high-κ gate oxide layer [17, 35]. In addition, anodisation process allows optimising surface morphology and properties by controlling anodisation parameters such as anodisation voltage, anodisation duration, electrolyte concentration, electrolyte pH, and electrolyte temperatures [33, 37]. The surface morphology and crystallinity of gate oxide films are strongly depending on the anodisation process variables.

Recently, the effects of anodisation durations of sputtered Sm/Si system have been investigated and reported [37]. According to this reported work [37], it was found that the optimised anodisation duration was 10 min. However, the obtained dielectric constants were low. The anodisation process of sputtered Sm on Si was carried out at a fixed voltage of 20 V in 1 M NaOH solution with pH value of 14. The strong base NaOH solution may cause excessive reaction and produce remnants [38]. Therefore, in this Letter, we investigate the influence of applied voltage (10–25 V) on physical and electrical properties of anodic Sm_2O_3 film on Si in lower pH of 11 of 0.01 M NaOH solution.

2. Experimental procedures: The cleaned 1 cm^2 Si substrates [*n*-type, (100)-oriented, 1-10 Ωcm] were placed at distance of 20 cm under the Sm target (Kurt J. Lesker, USA, 99.9% purity) in the RF magnetron TF 450 physical vapour deposition sputtering system to deposit 15 nm of samarium thin film, under working pressure of 3×10^{-3} Pa and power of 170 W. Sputtering process was carried out under pure argon medium with the flow rate of 25 cm^3 min^{-1} at room temperature. Sm-sputtered Si substrate was attached on the copper holder by sliver paste and connected to the negative terminal (anode) of GW Instek GPS-30300, DC power supplies; whereas the positive terminal (cathode) was connected to a platinum electrode. The electrolyte used was 0.01 M NaOH (pH = 11). The applied voltage was varied for a set of formation voltage (10, 15, 20, and 25 V) and holding for 10 min. As-anodised samples were rinsed with deionised water and dried in N_2 stream.

PANalytical Empyrean X-ray diffractometer (XRD) system in a scan rage of $2\theta = 20$–$90°$ was used to identify film crystallinity. The cross-sectioned film was analysed by TECNAI G2 F20 high-resolution transmission electron microscope (HRTEM). Prior to this, Pt was deposited on samples surfaces to protect the surface from ion bombardment damage caused by focused ion beam during lamella preparation.

Prior to the electrical characterisation, the Sm_2O_3 films were fabricated into metal–oxide–semiconductor (MOS) capacitor with an area of 3×3 mm^2 of electrode contact area. Al layer of 100 nm thickness was thermally evaporated on the top of the film as gate electrode by using thermal evaporator under vacuum system of 3×10^{-3} Pa. The 20 A of current is applied to heat up the tungsten coil and melt the aluminium. The evaporated Al was condensed on top of the surface of sample through a strip mask and backside of Si as Ohmic back contact. High frequency (1 MHz) and applied DC voltage of 24 mV was introduced to fabricated capacitor. MOS capacitance was measured by Hewlett Packard 4194A Impedance/Gain-Phase Analyser. Bias sweep was done in forward and backward cycle ranging from −5 to +1 V. The current–voltage (*I–V*) measurement was done at the frequency of 50 Hz and sweep mode was set at the range from 0 to 20 V using Keithley Instruments Model 236 Source Measure Unit.

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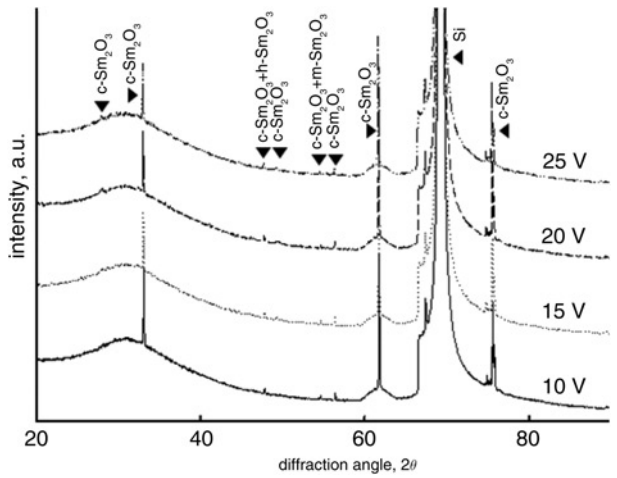

Fig. 1 *XRD pattern of anodised Sm_2O_3 at various applied voltages (10–25 V) on Si substrate*

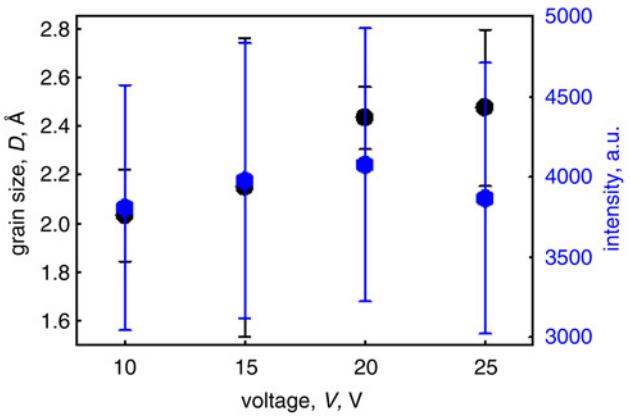

Fig. 3 *Grain size and intensity of hexagonal-Sm_2O_3 ($2\theta = 47.8°$) and monoclinic-Sm_2O_3 ($2\theta = 54.5°$) at various applied voltages (10–25 V). The error bars indicate the maximum and minimum of grain size and intensity, respectively*

3. Results and discussions: Fig. 1 shows the XRD pattern of anodised Sm_2O_3 film at various applied voltages (10–25 V) on Si substrates. According to International Centre for Diffraction Data (ICDD) card number 98-003-3650, cubic-Sm_2O_3 appeared at $2\theta = 27.8°$, 33.0°, 47.8°, 49.5°, 54.5°, 56.4°, 61.7°, and 75.6° in small concentration (relative intensity ; 0.01–0.25%) as compared with the strong Si substrate peak at 69.2° [23, 24]. Besides that, the two diffraction peaks at $2\theta = 47.8°$ and 54.5° are associated with hexagonal-Sm_2O_3 and monoclinic-Sm_2O_3, respectively. The peak intensity of 20 V sample is the highest and all the cubic-Sm_2O_3 can be observed distinctively. With further increase of the anodisation voltage to 25 V, the peak intensity is reduced significantly. The peak intensity of Sm_2O_3 is reduced may be due to more oxygen atoms diffused to Sm/Si interface from Sm_2O_3 film when higher anodisation voltage is applied. Owing to this reason, the thicker Sm silicates are formed but Sm_2O_3 film become thinner [23]. The 20 V sample contained the highest Sm_2O_3 average peaks intensity (16564.8 a.u.) and the smallest grain size with the average of 1.55 Å. The grain size of the cubic-Sm_2O_3 can be obtained through Scherrer equation [23, 24]

$$D = \frac{K\lambda}{\beta \cos\theta} \tag{1}$$

where D is the grain size, K is the shape factor (~0.9), λ is the X-ray wavelength, β is the line broadening at full width at half maximum, and θ is the Bragg angle. Smaller grain size will aid in electro-migration effects and resulted in decreasing current density.

Fig. 2 presents the grain sizes and intensities of cubic-Sm_2O_3 at various applied voltages (10–25 V), based on the three highest peaks, $2\theta = 33.0°$, 61.7°, and 75.6°. While Fig. 3 shows the grain sizes and intensities of mixture hexagonal and cubic Sm_2O_3 ($2\theta = 47.8°$) and monoclinic and cubic Sm_2O_3 ($2\theta = 54.5°$) at various voltages (10–25 V). Additionally, the intensity profile of Fig. 3 showed similar trend as Fig. 2, as Sm_2O_3 thin film anodised for 20 V has the highest intensity of mixture hexagonal-cubic-Sm_2O_3 and monoclinic-cubic-Sm_2O_3 peaks and the lowest peaks intensity is 25 V anodisation. However, the grain size increased as the anodisation voltage increased, this might be due to the fact that monoclinic crystalline structure is easier to form at higher energy system. Grain size of mixture monoclinic- and hexagonal-Sm_2O_3 for 20 V anodisation is considerably high as compared with 10 and 15 V anodisation, with the average grain size of 2.44 Å, which provided better electrical properties due to highest intensity of monoclinic-cubic-Sm_2O_3 peak at $2\theta = 54.5°$ (3472.40 a.u.). Fig. 4 shows the cross-sectional HRTEM images of the 20 V sample with 10 min of anodisation. It is assumed that same gate oxide thickness for different applied voltages [34]. The total oxide layer thickness is 17 nm while the Sm_2O_3 film is 14 nm. However, a 3 nm interface layer ($Sm_xSi_yO_z$) are formed between the Sm_2O_3 film and Si substrate.

The C–V characteristic graph of Sm_2O_3–Si MOS anodised at various voltages (10–25 V) in Fig. 5 shows the increasing trend

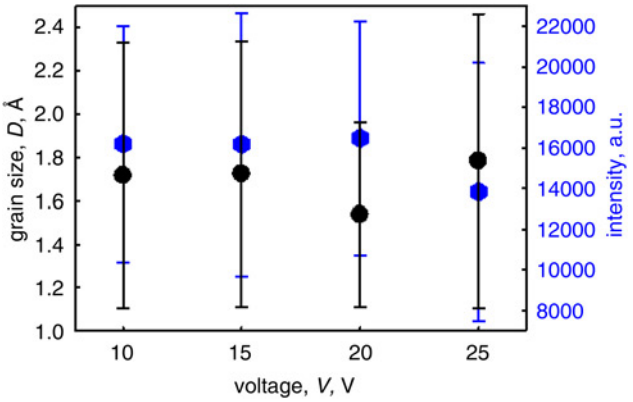

Fig. 2 *Grain size and intensity of cubic-Sm_2O_3 at various applied voltages (10–25 V). (Based on the three highest peak, $2\theta = 33.0°$, 61.7°, and 75.6°). The error bars indicate the maximum and minimum of grain size and intensity, respectively*

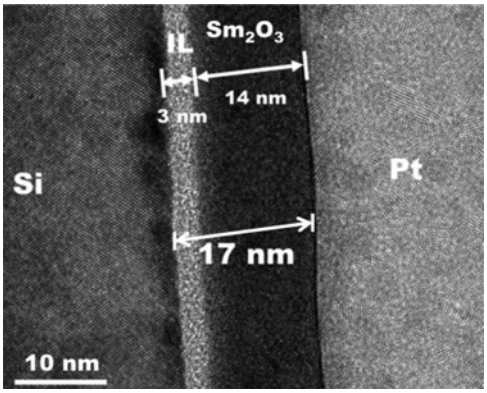

Fig. 4 *Cross-sectional HRTEM images for 20 V sample. Pt is used as protective layer during lamella preparation before HRTEM and EDX analysis*

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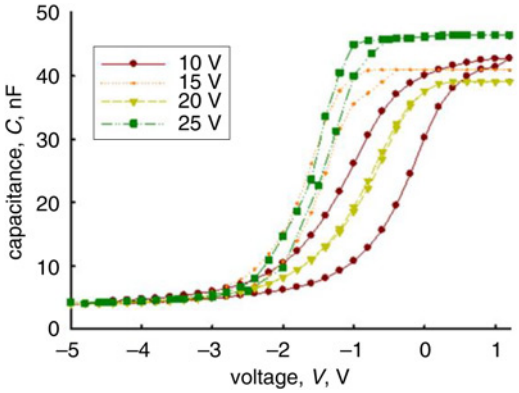

Fig. 5 *C–V characteristics of Sm_2O_3–Si MOS at various applied voltages (10–25 V)*

from 10 V and reached its threshold at 20 V. The highest oxide capacitance, C_{ox} obtained was 48.05 nF corresponding to sample anodised at 25 V. According to (2), the higher oxide capacitance of 25 V may be due to thinness of Sm_2O_3 film as inferred in XRD analysis

$$C_{ox} = \frac{\kappa_{ox}\varepsilon_o A_{ox}}{t_{ox}} \tag{2}$$

where C_{ox} is the oxide capacitance, κ_{ox} are dielectric constant for high-κ oxide and gate oxide, respectively, ε_o is permittivity of free space, A_{ox} is the area, and t_{ox} is the thickness of gate oxide [1, 9].

Fig. 6 displays the dielectric constant of Sm_2O_3–Si MOS produced at various applied voltages (10–25 V) with 10 min of anodisation duration. The highest k value was attained by 25 V anodised sample. The attained dielectric constants for all the anodised samples range from 8.11 to 10.30. However, these obtained values are lower as compared with the reported literature values of ~15 [14, 18–25]. This might be due to the extremely high value of Q_{eff}, STD, D_{it}, and D_{total}, charges are trapped in Si metal, IL and less charge are transmitted to the Al gate, and thus the dielectric values are lower as compared with the literature values.

Fig. 7 shows the effective oxide charge of Sm_2O_3–Si MOS at various applied voltage (10–25 V) with 10 min of anodisation. Fig. 8 is the graph regarding slow trap density of Sm_2O_3–Si MOS at various applied voltages (10–25 V) with 10 min of anodisation. The 20 V sample achieved the lowest Q_{eff} (2.78×10^{23} cm^{-2}) and STD value (2.91×10^{22} cm^{-2}), which enables more effective charges/carriers transferred in the MOS system.

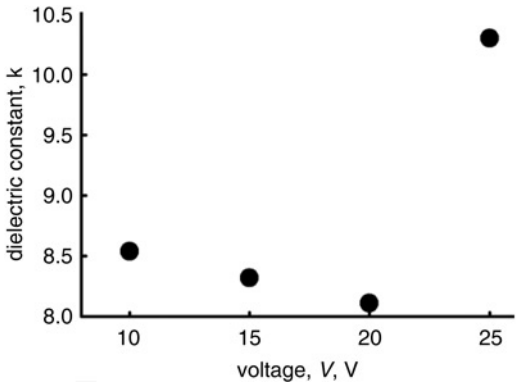

Fig. 6 *Dielectric constant of Sm_2O_3–Si MOS at various applied voltages (10–25 V)*

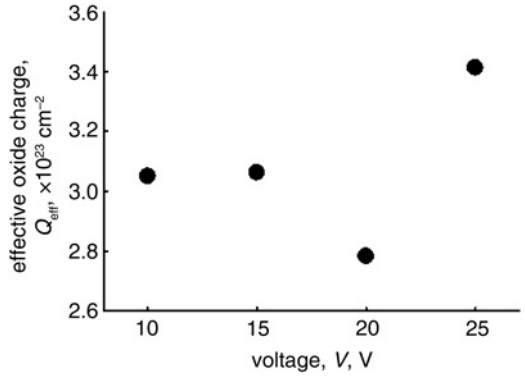

Fig. 7 *Effective oxide charge of Sm_2O_3–Si MOS at various applied voltages (10–25 V)*

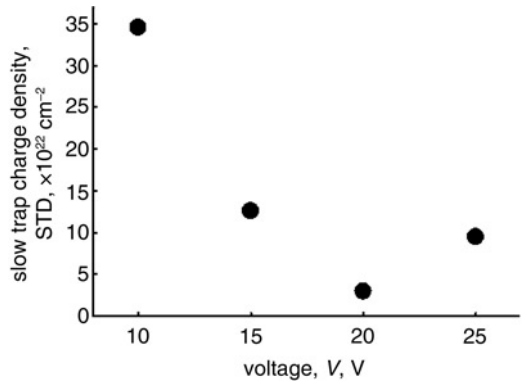

Fig. 8 *Slow trap density of Sm_2O_3–Si MOS at various applied voltages (10–25 V)*

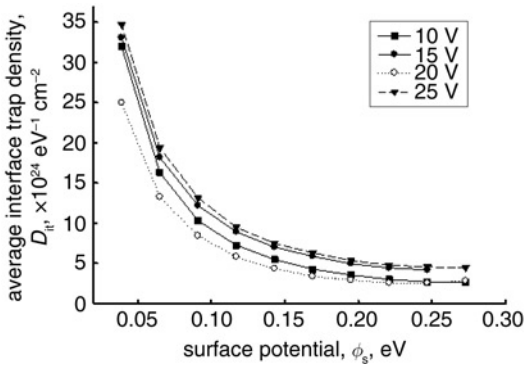

Fig. 9 *Average interface-trap density of Sm_2O_3–Si MOS at various applied voltages (10–25 V)*

Fig. 9 showed the average interface-trap density of Sm_2O_3–Si MOS at various applied voltage (10–25 V) with 10 min of anodisation by applying (3) as follows [9]

$$D_{it} = \frac{\Delta V_g C_{ox}}{\varphi_s q A} \tag{3}$$

where φ_s is the surface potential of Si at specific gate voltage, V_g. The value of D_{it} obtained in this work is ~10^{24} $eV^{-1}cm^{-2}$ at φ_s in the range of 0.039–0.273 eV.

Fig. 10 is the J–E measurement of Sm_2O_3–Si MOS at various applied voltages (10–25 V) with 10 min of anodisation. Anodisation voltage of 15 and 20 V indicate two-step dielectric

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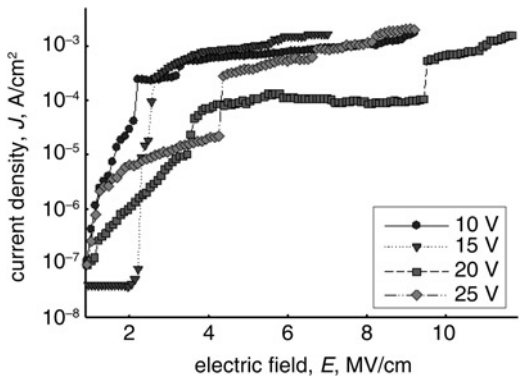

Fig. 10 *J–E measurement of Sm_2O_3–Si MOS at various applied voltages (10–25 V)*

Table 1 Summary of thickness, dielectric constant, leakage current density, and electrical breakdown field of Sm_2O_3 films deposited by various methods

Deposition method	Thickness, nm	κ	J, A cm^{-2}	E, MV cm^{-1}	Ref.
RF sputtering	25	—	$\sim10^{-3}$	15	[14]
RF sputtering	7.5–8.2	14.3	$\sim10^{-7}$	—	[20]
RF sputtering	61	—	$\sim10^{-6}$	—	[31]
DC sputtering	120	10.4	$\sim10^{-7}$	—	[21]
thermal evaporation	122.2	42.7	—	—	[28]
resistive evaporation	—	13	–	7	[30]
PLD	61.4	—	$\sim10^{-8}$	0.2	[27]
atomic layer deposition	50	10	1.1×10^{-8}	0.38	[18]
sputtering + anodisation	17	8.11–10.30	$\sim10^{-4}$	9.5	this work

breakdown. However, the breakdown voltage in 20 V is higher than the second breakdown voltage of 15 V, which is able to withstand highest electric field and breakdown only at 3.48 MV/cm at 10^{-5} A/cm^2 (first breakdown) and 9.50 MV/cm at 10^{-4} A/cm^2 (second breakdown). As summarised in Table 1, Kao *et al.* [14] reported a higher breakdown field of 15 MV/cm as compared with this work; however, larger leakage current of one order of magnitude was also recorded as compared with this work. Besides that, 15 V of anodisation voltage shows unstable breakdown, this might be due to instantaneous increment of current density or fluctuation voltage at the beginning.

4. Conclusion: The Sm_2O_3 film was successfully produced by anodisation of sputtered Sm/Si system. The sample anodised at 20 V demonstrated the highest electrical breakdown field of 9.50 MV/cm at 10^{-4} A/cm^2. This is attributed to the lowest effective oxide charge, slow trap charge density, average interface trap density, and total interface trap density.

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