Real Time Implementation of 3-Phase 4-Wire Shunt Hybrid Active Power Filter Based on PI Controller
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Reference

ABSTRACT
This paper presents an active and reactive (D-Q) current control method to generate the required reference current for three phase four wire shunt hybrid active filter (SHAPF) to solve power system network problems. Here, the passive elements of SHAPF have been used for compensation of reactive power and lower order harmonics and the active part mitigates the higher order harmonics. A modified phase lock loop has been used to handle the double frequency element of non-ideal voltages. A PI controller is used in the DC voltage loop for minimization of unwanted power loss inside the inverter. The simulation has been conducted in MATLAB/SIMULINK environment for ideal and unbalanced mains voltage condition. A laboratory prototype has been built on dSPACE1104 platform to verify the feasibility of the suggested SHAPF controller. From the simulation and experimental results the robustness of the proposed SHAPF controller has been proved.

Keywords
active power filter, harmonic compensation, phase lock loop (PLL), PI controller, synchronous reference frame (SRF) method, total harmonic distortion (THD)
Nomenclature

\[ d-q = \text{direct axis-quadrature axis} \]
\[ I_{d},V_{q_0} = \text{filter current, Quadrature axis side source} \]
\[ V_{abc} = \text{three phase source voltage} \]
\[ V^{+},V^{-},V^{0} = \text{positive, negative, and zero sequence source} \]
\[ \alpha,\beta = \text{axis for Clarke transform} \]
\[ \theta^{+},\theta^{-} = \text{positive and negative sequence voltage phase} \]
\[ \theta = \text{estimated phase angle} \]
\[ \tau = \text{time constant of low pass filter} \]
\[ \omega = \text{natural frequency} \]
\[ \omega_{dc} = \text{transformation angle} \]

Introduction

Nowadays, the issues for non-linear equipment relating to power quality are becoming stronger. They are more sensitive and the systems are being contaminated more and more due to their usage. These harmonics interfere with sensitive electronic equipment and cause undesired power losses in electrical equipment [1-3]. In order to solve the power quality problem and to deliver clean power several methods have been proposed and developed by the researchers [4].

Passive filters that work as the least impedance path to tune harmonic frequencies, are simple and less expensive but have several drawbacks including fixed compensation, they are bulky devices and the resonance problem of the L-C filters; however, APF has been developed for complete compensation of distortions [5]. Owing to the rapid improvement in power semiconductor device technology, active power filters have been considered as an effective solution for the power quality issue. The APFs use power electronic converters that insert harmonic components into the electrical network that cancel out nonlinear load harmonic currents. With the harmonic compensating ability, APFs are also capable of reactive power reduction and balancing the unbalanced load [6,7]. Although different types of active filters have been proposed to increase the electric system quality, pure APF is limited due to its high cost and rating constraints by power devices. To make the active filter smaller, cheaper and more practicable in industrial applications, a hybrid configuration of the active power filter appears very attractive in power distribution networks. However, Series Hybrid active power filters are complex, unreliable, and expensive. Therefore, a Shunt Hybrid filter topology is characterized by a combination of a parallel-connected passive filter and a small rated active filter [8]. This has been considered in this paper for its capability of attenuation and effective operation. Since the development of APFs, various control schemes, such as fast Fourier transform (FFT); recursive discrete Fourier transform (RDFT); instantaneous active and reactive power (p-q); direct testing and calculating (DTC) method; instantaneous active and reactive current component (i_d,i_q) [9]; notch filter, sine multiplication, generalized integral, synchronous detection algorithm; adaptive filter, flux based controller; artificial neural network (ANN); adaptive linear neuron (ADALINE); wavelet transform; particle swarm optimization (PSO); and genetic algorithm (GA) techniques have been proposed in the literature [10,11]. Among these control schemes, SRF is one of the most conventional and practically applicable methods [12,13]. Although it performs an excellent job, it requires a PLL circuit for synchronization. Different types of PLL have been introduced in the literature [14]; however, the conventional types of PLL have low performance in extremely unbalanced and distorted networks. So, this paper is aimed at the competency of the SRF method with the modified PLL.

This paper presents a new technique based on SRF method using the modified PLL algorithm and compares its performance with that of conventional SRF method and P-Q theory under balance and unbalance condition. In the proposed control method for SHAPF is optimized without using load voltage and source current measurement. So that the numbers of measurements are reduced and system performance is improved. A hysteresis controller is adopted here to generate the switching signals for voltage source inverter. DC-link voltage regulator, basically comprised of a PI controller, can minimize the switching losses occurring in VSI. To find out PI controller gains for mitigation of harmonics optimally equations with some parameters have been taken under consideration. The proposed algorithm is simple and easy to implement; therefore, it can be run efficiently in DSP platforms. During the last years, due to high performances and computation facilities in power conditioning applications the DSP-based control has become increasingly widespread [15]. Current-control techniques based on DSP for three-phase SAPFs are given in Ref. [16] as a comprehensive comparison of different high-performance. Additionally, developing a real-time systems theory is a most concern. In this context, it is a convenient solution to implement the proposed control algorithm through dSPACE platforms [17] as a prototype based on versatile controller board DS1104.

The structure of this paper is as follows: the hybrid active power filter is discussed in the second section. The third section describes the control algorithm of APF. The simulation results and a brief analysis are presented in the fourth section. In the fifth section, experimental results are shown. Finally, conclusions are drawn in the sixth section.
Hybrid Active Power Filter Topology

The proposed hybrid filter structure shown in Fig. 1 comprises a shunt passive filter and shunt active filter. A 3-leg inverter with split capacitor works as the APF. It is designed to be associated in parallel with the single phase and three phase loads that are considered as a non-linear and unbalanced load for a 3-phase 4-wire distribution system, while its complex control circuitry and massive DC link capacitors are necessary for perfect operation. The inner point of every branch is attached to the power network through an inductor, which is used to filter the ripples of inverter current. The considered LC passive filter at the fifth harmonic tuned frequency is connected in shunt to the power line before the load. This provides a low impedance trap for harmonics to which the filter is tuned, and, correspondingly, aids in reduction of the active filter power rating.

Proposed Control Algorithm

The control strategy is an essential part for the proper and efficient operation of HAPF. To distinguish the load harmonic current and to inoculate the compensating current into the power system together with the current, but in the opposite phase distortion, is the basic operating principle of the APF. Hence, the APF can regulate and ensure that the current that is drawn at the common coupling point will be sinusoidal.

MODIFIED PLL OPERATION

To extract the voltage peak and instantaneous phase information, the best method is to convert the three phase unbalanced voltage in a 2D stationary frame. If this transformed voltage vector is drawn on a q-d frame, a circular vector rotating at speed equal to the frequency is seen for balanced case. Thus, if a transformed unbalanced voltage vector is drawn, an eclipse is formed as a resultant of both positive and negative sequence components. Suppose the frequency and phase information are already known and taking an arbitrary frame that is rotating in the same direction as that of a positive sequence component and at a speed equal to the frequency; then, a positive sequence component appears as a stationary and negative sequence component that seems to be rotating at a speed twice that of the frequency. For safe and consistent operation of an active power filter in an unbalanced and distorted grid voltage, the frequency and phase extraction of the positive sequence component of the voltage should be obtained quickly and accurately. Because of the dynamic behavior, conventional SRF-PLL performance is unsatisfactory under non-ideal voltage mains [19]. The improved PLL developed in this study is shown in Fig. 2, which is put forward for the determination of positive sequence components with stability and rapidity. For non-ideal mains voltage:

$$\begin{align*}
V_{sabc} &= \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} V_a^+ \\ V_b^+ \\ V_c^+ \end{bmatrix} + \begin{bmatrix} V_a^- \\ V_b^- \\ V_c^- \end{bmatrix} (1) \\
&= V^+ \begin{bmatrix} \sin(\theta^+ - 2\pi/3) \\ \sin(\theta^+ + 2\pi/3) \end{bmatrix} + V^- \begin{bmatrix} \sin(\theta^- + 2\pi/3) \\ \sin(\theta^- - 2\pi/3) \end{bmatrix} + V_0 (2)
\end{align*}$$

FIG. 1 Schematic diagram of 3-phase 4-wire SHAPF [18].
Using $z/\beta$ transform, the voltage vectors are:

$$V_{z/\beta} = \begin{bmatrix} V_x \\ V_\beta \end{bmatrix} = [T_{z/\beta}] V_{abc} \tag{3}$$

where:

$$[T_{z/\beta}] = \begin{bmatrix} 1 & -1 \\ 2/\sqrt{3} & 2/\sqrt{3} \end{bmatrix}$$

So:

$$V_{z/\beta} = \begin{bmatrix} V_x \\ V_\beta \end{bmatrix} = \begin{bmatrix} V^+ \sin \theta^+ + V^- \sin \theta^- \\ -V^+ \cos \theta^+ + V^- \cos \theta^- \end{bmatrix} \tag{4}$$

Performing d-q transform:

$$V_{dq} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} = [T_{dq}] V_{z/\beta}$$

where:

$$sT$$

is the time constant of the low pass filter.

PLL successfully tracks the phase at $\hat{\theta} = \theta^+ = \theta^-$. So

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} \approx \begin{bmatrix} V^- \sin(2\hat{\theta}) \\ -V^+ + V^- \cos(2\hat{\theta}) \end{bmatrix} \tag{6}$$

Here, $2\hat{\theta}$ is the double frequency to be eliminated. It is the basic concept of the modified PLL structure. It can provide the positive sequence component by cancellation of $2\omega$ oscillations [20]. The waveforms of transformation angle based on conventional and modified PLL algorithms are illustrated in Fig. 3. The modified PLL circuit uses Clarke and Park transform for identifying the peak of positive sequence voltage. The unbalanced voltages are converted to the stationary coordinate system. Through the measured phase angle, the voltages in stationary co-ordination are transformed to the d-q frame. The PI controller forced the d-axis component $V_d$ to zero so as to align the mains voltage space vector with the q-axis. The estimated phase angle $\hat{\theta}$, which is attained by integrating the PI controller output, is, in turn, used for the coordinate transformation process [21]. Here, a second order resonant filter is used instead of the conventional low pass filter for suppressing the double fundamental frequency, which is created for unbalancing and the gain adaptation block shows the convergence of any value of system voltages and creates normalized templates of fundamental voltage [22]. The rate limiter block works as an attenuator against the ripple. The modified PLL can perform satisfactorily as long as the gains of the PI are adjusted accordingly under highly inaccurate and disturbed system voltages.

The transfer function of the resonant filter is given in:

$$H(s) = \frac{s^2 + 4\omega^2}{s^2 + 4\omega_{cut-off}^2 + 4\omega^2} \tag{7}$$

and the open loop PLL gain is written as:

$$G(S) = V \cdot \frac{1}{s} \cdot kp \cdot \left(1 + \frac{1}{sT}\right) \cdot H(s) \tag{8}$$

where $T$ and $k_p$ are the time constant and gain of the PI controller correspondingly. Now a critically damped system is considered and the value of the cut-off frequency is chosen as it is equal to double the fundamental frequency [23]. For selection of the PI controller gains, the resonant filter is approximated as a low pass filter and the parameter design is obtained via optimum symmetrical method:

$$T = 4\tau \tag{9}$$

$$k_p = \frac{1}{2V\tau} \tag{10}$$

where $\tau$ is the time constant of the low pass filter.

---

**FIG. 3**

Waveforms of transformation angle for the (a) conventional and (b) modified PLL algorithms.
Accordingly, the transformation angle waveforms in simulation for conventional SRF-PLL and the modified PLL are shown in Fig. 4. The modified PLL performed better than the previous one, since the output has low oscillations under non-ideal supply conditions. As the resonant filter and PI controller are present, there is some phase delay of the signal, which offers a very high attenuation to double the fundamental frequency component in the d-axis grid voltage due to unbalancing.

REFERENCE CURRENT GENERATION

The three phase load currents are measured using a hall-effect current sensor and converted into d-q-0 by means of a rotational frame that is synchronous with the system voltage positive sequence in Eq 11.

\[
\begin{bmatrix}
  i_d \\
  i_q \\
  i_0
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
  \sin(\omega_s t) & \sin(\omega_s t - \frac{2\pi}{3}) & \sin(\omega_s t + \frac{2\pi}{3}) \\
  \cos(\omega_s t) & \cos(\omega_s t - \frac{2\pi}{3}) & \cos(\omega_s t + \frac{2\pi}{3}) \\
  \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}
\end{bmatrix} \begin{bmatrix}
  I_{La} \\
  I_{Lb} \\
  I_{Lc}
\end{bmatrix}
\]

where \(\omega_s\) is considered here as the transformation-angle of the positive sequence source voltage and is delivered by the phase lock loop [24].

The system under observation is a three phase-four wire in which the active component \(i_d\) and oscillating part \(i_q\) are reflected. After the load currents \(i_d\) and \(i_q\) are found, they are allowed to pass over a low pass filter to separate the AC and DC part through which the active and reactive fundamental current components \((i_{d-DC}, i_{q-AC})\) are obtained. Both the currents \((i_{d-DC}, i_{q-AC})\) AC parts are related with the responsibility for active and non-active harmonic components. The filters used in the circuit are the second order Butterworth type and their cut off frequency is identical to one half of the fundamental frequency [25]. In consideration of reactive current, the passive filter provides its DC value, whereas the VSI delivers an AC voltage to sink the harmonics. The filtered active and non-active currents from Eq 12 are used for generation of the accurate references to the modulator:

\[
\begin{bmatrix}
  i_d & AC \\
  i_q & AC
\end{bmatrix} = \begin{bmatrix}
  i_d \\
  i_q
\end{bmatrix} - \begin{bmatrix}
  i_d & DC \\
  i_q & DC
\end{bmatrix}
\]

As well as providing harmonic currents, the DC voltage of the PWM VSI should be maintained for accurate operation. The voltage of the capacitor is controlled by regulating the reactive current, as shown in Fig. 4 [17]. Then the a-b-c frame reference currents are:

\[
\begin{bmatrix}
  i_d \\
  i_q \\
  i_r
\end{bmatrix} = \begin{bmatrix}
  \sin(\omega_s t) & \cos(\omega_s t) \\
  \sin(\omega_s t - \frac{2\pi}{3}) & \cos(\omega_s t - \frac{2\pi}{3}) \\
  \sin(\omega_s t + \frac{2\pi}{3}) & \cos(\omega_s t + \frac{2\pi}{3})
\end{bmatrix} \begin{bmatrix}
  i_d & AC \\
  i_q & DC
\end{bmatrix}
\]
DC LINK CAPACITOR VOLTAGE CONTROL
The DC voltage can build up in the APF and is regulated across the DC capacitors by itself [26]. The selection of DC value confirms that the current time derivatives of the converter supply are required for compensation of the selected harmonics. Using this concept the capacitor voltage is chosen from:

$$C_{dc} = \frac{\pi I_f}{\sqrt{3} \cdot \omega \cdot V_{dc(p-p)} \cdot \text{max}}$$

In order to control the inverter current actively the nominal DC bus voltage $V_{dc}$ should be larger or identical to the line-line peak voltage [27]. According to the capacity of the system it can be selected as $V_S < V_{dc} \leq 2V_S$.

PI-Controller
The internal composition of the PI control circuit is exposed in Fig. 5. The actual DC-side capacitor voltage of the shunt active filter is sensed through a hall-effect voltage sensor and compared with a reference set DC voltage. The comparison result of the voltage error at the nth sampling instant, error = $V_{dc, ref} - V_{dc}$ is passed to the PI controller. The transfer function $H(s) = k_p + k_i/s$ is defined for it [28]. For the determination of the dynamic response of the measured voltage the following equations are used:

$$k_p = 2\xi \omega_n c \cdot k_p \cdot 0.5$$

$$k_i = \alpha \omega_n c \cdot k_i \cdot 1.5$$

The proportional gain is derived from Eq 15. Similarly, the integral gain is achieved by using Eq 16, which fixes the steady state error, and the settling time in the DC-side capacitor voltage is eliminated. The peak reference current magnitude, $I_{max}$ is estimated via this controller and the DC-side capacitor is controlled [29].

REACTIVE POWER CONTROL
It is essential to arrange the unity power factor for fundamental components at the terminals of the active filter. Since $Q = 3/2V_{qd}I_{dh}$ is the expression of the reactive power it can be accomplished by keeping the $d$-axis current at zero [30]. The above control combination generates the required active power filter output fundamental current [31].

HARMONIC CURRENT GENERATOR
A hysteresis comparator is used here for a quick response and appropriate sinusoidal current tracking capability. The desired current, $I_f(t)$ and the injected inverter current, $I_{ref}(t)$ are compared with one another. The logic of switching is as followed:

If $I_f < (I_{ref} - hb)$ upper switch S1 is OFF & lower switch S6 is ON in leg of “a” of active power filter.

If $I_f > (I_{ref} + hb)$ upper switch S1 is ON & lower switch S6 is OFF in leg of “a” of active power filter. Correspondingly, in the legs “b” & “c” the switches are initiated. Here “hb” is the hysteresis band and determines the variation of load current harmonics and switching frequency of the devices.

Simulation Results and Analysis
The performance of a 3-legs 4-wire Hybrid active power filter for filtering current distortions, compensation of neutral current, load current balancing, and reactive power mitigation has been examined under these conditions: balanced source-balanced load, unbalanced source-balanced load, and balance source-unbalance load. The goal of this case study is to
demonstrate the validity and evaluation of the proposed approach, where the source is greatly unbalanced.

Using the power system blockset in MATLAB-Simulink for a three phase four-wire power network with shunt active and shunt passive filter the presented simulation results are obtained. The results are specified in the following simulation studies for before compensation, compensation using only passive filter, and after the operation of the hybrid filter. Three and single phase diode rectifier nonlinear loads are coupled in the power system for producing unbalanced, reactive current and harmonics in the load current as well as neutral current. The widespread simulation outcomes are discussed below.

**BALANCE SOURCE CONDITION**

Considering the balanced source and balanced load case, the proposed controller shows the effective results for compensation of the current harmonics. The simulation time is taken as $t = 4.9$ to $t = 5$ s in steady state condition with constant load. The source voltage is shown in Fig. 6(a). The load current and its FFT spectrum is given in Fig. 6(b) and 6(c), which is highly non-linear in nature. After the application of the passive filter, although the lower order harmonics are reduced, the non-linearity and distortion still exists, this is presented in Fig. 6(d). The source current after insertion of the active filter total compensation with PI controller is as shown in Fig. 6(f). From Fig. 6(g) it is clear that the waveform becomes sinusoidal with some high frequency ripples. The voltage across the DC link capacitor settles down after a few cycles. The source current and their respective THD levels are summarized in Table 1.

**UNBALANCED SOURCE CONDITION**

Voltage unbalance occurs when the relative magnitudes and phase angle of the three phases are not equal. The source voltage magnitude of phase-b is 20% smaller than the source voltage of phase-a, and the phase-c voltage is 50% lower than phase-a. This is done by using a three phase programmable voltage source block in Simulink. The negative sequence fundamental voltage component is inserted here to create an unbalance in the system voltages. The three phase unbalanced voltages are considered as: $V_{sa} = 100 \sin \omega t$, $V_{sb} = 80 \sin (\omega t - 120)$ and $V_{sc} = 50 \sin (\omega t + 120)$. Zero sequence power is required for the non-linear load as both source voltages and load currents are unbalanced. When there is an unbalance in the supply voltages, the fundamental components are first derived using PLL to make the unit templates for the balanced and sinusoidal voltages. Then the synchronizing phase angle is extracted and simulation is performed through it. The source voltage is shown in Fig. 7(a). The load current and its FFT graph without compensation are given in Fig. 7(b) and 7(c), which is highly non-linear in nature. After the application of the passive filter lower order harmonics are reduced but non-linearity and
TABLE 1  Simulation results for balanced and unbalanced voltage condition.

<table>
<thead>
<tr>
<th>Source Current</th>
<th>Before Filter</th>
<th>Passive Filter</th>
<th>Hybrid Active Filter</th>
<th>Before Filter</th>
<th>Passive Filter</th>
<th>Hybrid Active Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD (%)</td>
<td>Balance Voltage</td>
<td>Unbalance Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A-phase</td>
<td>27.67</td>
<td>7.78</td>
<td>2.06</td>
<td>21.07</td>
<td>14.69</td>
<td>3.31</td>
</tr>
<tr>
<td>B-phase</td>
<td>27.65</td>
<td>7.80</td>
<td>2.29</td>
<td>48.59</td>
<td>27.11</td>
<td>3.71</td>
</tr>
<tr>
<td>C-phase</td>
<td>27.78</td>
<td>7.79</td>
<td>2.25</td>
<td>21.18</td>
<td>10.64</td>
<td>3.14</td>
</tr>
<tr>
<td>RMS(A)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A-phase</td>
<td>1.29</td>
<td>1.98</td>
<td>3.21</td>
<td>1.12</td>
<td>1.64</td>
<td>3.97</td>
</tr>
<tr>
<td>B-phase</td>
<td>1.23</td>
<td>1.96</td>
<td>3.31</td>
<td>0.87</td>
<td>2.41</td>
<td>3.84</td>
</tr>
<tr>
<td>C-phase</td>
<td>1.25</td>
<td>1.98</td>
<td>3.23</td>
<td>1.54</td>
<td>2.23</td>
<td>3.21</td>
</tr>
<tr>
<td>Neutral</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>5.25</td>
<td>—</td>
<td>1.43</td>
</tr>
</tbody>
</table>

distortion still exists, which is presented in Fig. 7(d). The source current after insertion of the active filter total compensation with PI controller is as shown in Fig. 7(f). It is determined from the responses that the settling time required by the PI controller is approximately 8 cycles. The THD of the source current is reduced from 21.07 to 3.31 % in the case of PI controller, which is below the IEEE standard for both controllers, as shown in Fig. 7(g). In Fig. 7(l), waveform of neutral current is shown. The summary of the source current and their THD levels are listed in Table 1. Although the load currents are not purely balanced they are satisfactory.

UNBALANCE LOAD CONDITION

Unbalance loading is the most prominent, and active filters should be designed to compensate the harmonics, reactive power and neutral current under unbalanced load condition. A single phase diode rectifier with RL load is connected across phase “c” to create an unbalanced load current. The feasibility of the proposed method is tested and the simulation results are presented in Fig. 8. The unbalanced load current and its harmonic spectrum before the installation of active power filter are shown in Fig. 8(b) and 8(c). When the shunt passive filter is introduced in the system, the THD level is reduced from 27.83 to 7.95 %, which is still beyond IEEE 519 standard (5 %). As soon as the shunt hybrid active power filter started operating, it compensates the source current harmonics to 2.88 %, which is shown in Fig. 8(g). From Fig. 8, it is seen that although the controller cannot totally balance the current, the results are quite satisfactory. The source currents are found to be sinusoidal, in phase with the respective voltages (near to unity power factor), as expected. DC link capacitor voltage is stable and follows the reference value. Moreover, the proposed control algorithm has the ability to compensate the excessive neutral current and it is shown in Fig. 8(f). Table 2 represents the summary of source current and their THD levels under unbalance load condition.

The gains of PI controller (Kp, Ki) have great influence over the elimination of the steady state and overshoot error in DC voltage. These also have an effect on controlling THD, real power and reactive power of SHAPF. To analyze the effects of PI controller, some cases have been taken into account where the stated cases are closely related and show good results. In Table 3, the values of different parameters are presented for different values of Kp and Ki gains of PI controller. For Kp = 0.5 and Ki = 1.5, the parameters obtained are already discussed previously, which are satisfactory. However, when Kp and Ki values are changed like Kp = 2, 4.2 and Ki = 2.8, 3.9 the performance of the SHAPF also changed. From Table 3, it has been seen that when Kp = 4.2 and Ki = 3.9, the THD values have become 3.57 and 3.92 % for balanced and unbalanced conditions, respectively, which are higher than the THD values for Kp = 0.5 and Ki = 1.5. For other parameters the same scenario has also been observed.

It has been observed that the shunt hybrid active power filter performance with PI controller shows outstanding characteristics compared to the conventional controller under any operating voltage condition. The calculation of real (P) and reactive (Q) power for different cases are arranged in Table 4. The parameters used in this study for the SHAPF system are listed in Table 5. In addition, a comparison between the proposed topology and Refs. [15,19] is shown in Table 6 in terms of THD % according to different conditions. The harmonic extraction algorithms are built on the same concept with a slight modification and the DC link voltage control is maintained through considering the active or reactive part of the filtered AC current. The THD values of the source current are significantly reduced when compared with the existing control techniques. Moreover, the proposed control scheme provides a faster response, and, concerning its operation, satisfactory performance is achieved.

Experimental Results

The system parameters selected for the experimental verification: Vs = 50 V (peak), f = 50HZ, Li = 5 mH, Lc = 5 mH, Rl = 100Ω, L1 = 20 mH, Cdc = 2000 μF, Vdc = 70 V. Parameters
FIG. 7 Simulation results for operational performance of SHAPF: (a) source voltage, (b) load current, (c) THD before compensation, (d) passive filtering source current, (e) THD after passive filtering, (f) source current after hybrid filtering, (g) THD after hybrid filtering, (h) injecting current, (i) DC link voltage, and (j) neutral current.

FIG. 8 Simulation results for operational performance of SHAPF: (a) source voltage, (b) load current, (c) THD before compensation, (d) passive filtering source current, (e) THD after passive filtering, (f) source current after hybrid filtering, (g) THD after hybrid filtering, (h) injecting current, (i) DC link voltage, and (j) neutral current.
of passive filter, $L_f = 3 \text{ mH}$, $C_f = 60 \mu \text{H}$. A prototype model of three-phase four wire APF is developed in the laboratory for experimentation shown in Fig. 9. There are two single-phase bridge inverters connected in series in each phase. Suitably designed snubber circuit is connected across each device. DC link capacitor is connected at the DC side of the inverter. Three coupling inductors are connected in series with the three lines on the AC side of the inverter. Three-phase diode rectifier with R-L elements on DC side is used as a nonlinear load, which draws nonlinear current. The AC and DC voltages are sensed using the isolation amplifier (AD202JN). The AC source currents are sensed using the PCB mounted Hall-effect current sensors (LEM-25-NP). The IGBT driver circuits are used for pulse amplification and isolation purposes. The driver circuit has special features like the fault protection and protection against the under-voltage lockout. The load current, the source voltage and injected filter currents, $i_{fabc}$ are measured. The sensed signals are used for processing in the designed control algorithm. Because real-time simulation is an important aspect for control engineering, the same is true for the automatic generation of real-time code, which can be implemented on the hardware.

### TABLE 2 Simulation results for unbalance load condition.

<table>
<thead>
<tr>
<th>Source Current</th>
<th>THD (%)</th>
<th>Neutral</th>
<th>C-phase</th>
<th>B-phase</th>
<th>A-phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD (%) Unbalance load</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A-phase</td>
<td>27.83</td>
<td>7.94</td>
<td>2.88</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B-phase</td>
<td>27.29</td>
<td>6.56</td>
<td>2.33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C-phase</td>
<td>28.58</td>
<td>7.47</td>
<td>2.42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RMS(A)</td>
<td>1.84</td>
<td>2.77</td>
<td>10.78</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### TABLE 3 Effect of PI controller parameter variation on SHAPF.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Balance Voltage</th>
<th>Unbalance Voltage</th>
<th>Unbalance Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_p = 0.5$, $K_i = 1.5$, Damping coefficient, $\xi = 0.7$, natural frequency, $\omega_n = 50 \text{ Hz}$</td>
<td>THD = 2.06 %, $V_{dc} = 220 \text{ V}$, Real power = 2.5 kW, Reactive power = 150 VAR</td>
<td>THD = 3.31 %, $V_{dc} = 220 \text{ V}$, Real power = 2.8 kW, Reactive power = 133 VAR</td>
<td>THD = 2.88 %, $V_{dc} = 220 \text{ V}$, Real power = 12 kW, Reactive power = 142 VAR</td>
</tr>
<tr>
<td>$K_p = 2$, $K_i = 2.8$ damping coefficient, $\xi = 0.5$, natural frequency, $\omega_n = 50 \text{ Hz}$</td>
<td>THD = 2.87 %, $V_{dc} = 219.2 \text{ V}$, Real power = 2.4 kW, Reactive power = 160 VAR</td>
<td>THD = 4.3 %, $V_{dc} = 218.7 \text{ V}$, Real power = 2.6 kW, Reactive power = 142 VAR</td>
<td>THD = 3.68 %, $V_{dc} = 220 \text{ V}$, Real power = 1.78 kW, Reactive power = 157 VAR</td>
</tr>
<tr>
<td>$K_p = 4.2$, $K_i = 3.9$ Damping coefficient, $\xi = 1$, natural frequency, $\omega_n = 50 \text{ Hz}$</td>
<td>THD = 3.57 %, $V_{dc} = 220 \text{ V}$, Real power = 2.42 kW, Reactive power = 155 VAR</td>
<td>THD = 4.92 %, $V_{dc} = 221.2 \text{ V}$, Real power = 2.67 kW, Reactive power = 148 VAR</td>
<td>THD = 4.21 %, $V_{dc} = 220 \text{ V}$, Real power = 2.5 kW, Reactive power = 201 VAR</td>
</tr>
</tbody>
</table>

### TABLE 4 PI controller performance evaluation.

<table>
<thead>
<tr>
<th>Condition</th>
<th>DC Voltage</th>
<th>P&amp;Q Without Active Filter</th>
<th>P&amp;Q With Active Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Balanced source</td>
<td>Settling Time = 0.29 s</td>
<td>800 W, 400 VAR</td>
<td>2.5 kW, 150VAR</td>
</tr>
<tr>
<td>Unbalanced source</td>
<td>Settling Time = 0.26 s</td>
<td>910 W, 370 VAR</td>
<td>2.8 kW, 133VAR</td>
</tr>
<tr>
<td>Unbalance load</td>
<td>Settling Time = 0.24 s</td>
<td>840 W, 350 VAR</td>
<td>2.67 kW, 142VAR</td>
</tr>
</tbody>
</table>

### BALANCE SOURCE CONDITION

The performance of the power inverter is first verified under balanced grid condition. Before turning on the inverter, source voltage is sinusoidal but load current is highly nonlinear in nature and its frequency spectrum measured by Fluke power quality analyzer is shown; its THD is 28.3 % for phase “a.” After using the fifth harmonic tuned passive filter, the value of the source current THD is reduced with 13.5 %. However, when the APF is connected in shunt with the line and passive filter, the source current waveform becomes sinusoidal. The THD of the source current of phase “a” after compensation is reduced to 4 %, which is shown in Fig. 10. As compared to simulation results, the experimental THD is slightly more due to the accuracy limit of sensors and sampling time limit of DSP of dSPACE. DC link voltage across the split capacitor is also stable and follows the reference value.

### UNBALANCE SOURCE CONDITION

The control algorithm is found to work satisfactorily under unbalanced source voltage conditions. Under unbalanced voltage conditions, a 14 % amplitude unbalance is introduced in the “b” and “c” phases so that the phase voltages are 50 V in phase “a,” 43 V in phase “b,” and 38 V in phase “c,” respectively. Fig. 11 shows the total response of the system for this condition. It is seen from the results that the control algorithm gives satisfactory results under unbalanced source voltages. It is shown in the figure that the load current waveform of phase “a” deformed...
before filtering. FFT result is also listed. After the operation of hybrid APF controlled by the PI controller Sinusoidal source, current waveform is obtained instantaneously after the insertion of active filter as illustrated in Fig. 11(f). Here, it is also shown that the experimental results of the DC-side capacitor voltage is nearly constant with small ripple. The current THD is reduced from 28 to 5 % for PI controller shown in Fig. 11.

**UNBALANCE LOAD CONDITION**

The Simulink model for the unbalanced load is built in the PC installed with MATLAB, which is integrated with dSPACE 1104 for real time implementation. Before turning on the inverter, the source voltage is sinusoidal, but the load current is highly nonlinear in nature and its frequency spectrum measured by Fluke power quality analyzer is shown; its THD is 23.3 % for phase “a.” After using the passive filter, the value of source current THD is reduced by 17 %. However, when the APF is connected in shunt with the line and passive filter, the harmonic contains in the source current is supplied by APF and the source current approaches to sinusoidal. The THD of the source current of phase “a” after compensation is reduced to 4.8 %, which is under the IEEE standard limit. The source current after the compensation and filter current is also shown in Fig. 12.

**Conclusion**

In this paper, a modified PLL is developed and employed effectively for grid voltage synchronization under balanced and unbalanced mains conditions. For computation of the reference current, the SRF theory has been described. It is shown that percentage of THD is reduced from 27.67 to 2.06 % for a balanced source, 21.07 to 3.31 % for an unbalanced source, and 27.83 to 2.88 % for an unbalance load. Moreover, 57 % amount of reactive power has been compensated after using the shunt hybrid APF. A laboratory prototype is developed and it has been found that value of THD has been reduced from 28 to 5 % for an unbalance voltage, 23.3 to 4.8 % for unbalance load, and 28.11 to 4 % for a balanced source, which is in the mark of 5 % specified in the IEEE-519 standard. Therefore, with the combination of PI and modified SRF theory approach, SHAPF can be considered as a reliable harmonic isolator for its quick response and good quality of filtering.
FIG. 10
Experimental results for balance source: (a) supply voltage, (b) load current before compensation, (c) %THD before compensation, (d) source current after passive filtering, (e) %THD after passive filter, (f) source current after compensation, and (g) %THD after SHAPF compensation.
FIG. 11
Experimental results for an unbalanced source: (a) supply voltage, (b) load current before compensation, (c) %THD before compensation, (d) source current after passive filtering, (e) %THD after passive filter, (f) source current after compensation, (g) %THD after SHAPF compensation, and (h) filter current.
FIG. 12
Experimental results for unbalanced load: (a) supply voltage, (b) load current before compensation, (c) %THD before compensation, (d) source current after passive filtering, (e) %THD after passive filter, (f) source current after compensation, (g) %THD after SHAPF compensation, and (h) filter current.
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References


