Influence of Design and Process Parameters of 32-nm Advanced-Process High-k p-MOSFETs on Negative-Bias Temperature Instability and Study of Defects

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Influence of Design and Process Parameters of 32-nm Advanced-Process High-\(k\) \(p\)-MOSFETs on Negative-Bias Temperature Instability and Study of Defects

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Negative-bias temperature instability (NBTI) has become a prominent factor limiting scaling of complementary metal–oxide–semiconductor technology. This work presents a comprehensive simulation study on the effects of critical design parameters of 32-nm advanced-process high-\(k\) \(p\)-channel metal–oxide–semiconductor field-effect transistors on NBTI. The NBTI mechanism and defects were explored for various geometric and process design parameters over a wide range of values. The NBTI simulation method applied in this work follows the on-the-fly method to capture the mechanisms of fast and slow traps. This work illustrates the dependence of the threshold voltage (\(V_{th}\)) degradation on the stress oxide field and stress temperature as well as investigation of the Arrhenius plot for the devices. The temperature insensitivity during short stress time of 1 ms indicates absence of generated defects and presence of preexisting defects. It is also observed that significant defects are generated in the gate stack subsequent to NBTI. The slope obtained from the \(V_{th}\) degradation analysis at 1 ks and 375°C shows that changing the SiO\(_2\) interfacial layer thickness affects the \(V_{th}\) degradation by 96.16% more than changing the HfO\(_2\) thickness and by 80.67% more than changing the metal gate thickness. It is also found that the NBTI effect depends on process design considerations, specifically the boron concentration in the highly doped drain, the metal gate work function, and the halo doping concentration; it was observed that higher boron dose and high metal work function may lead to higher \(V_{th}\) degradation. However, the halo doping concentration in the advanced 32-nm structure has an insignificant effect on NBTI.

Key words: High-\(k\), NBTI, defects, MOSFETs, reliability, degradation

INTRODUCTION

Over recent decades, miniaturization of metal–oxide–semiconductor field-effect transistor (MOSFET) devices has revolutionized the semiconductor industry, enabling production of extremely complex devices and systems. Scaling of MOSFET devices is important to achieve greater integration density, as compact transistors result in increased functionality, reduced power consumption, and faster switching time at reduced cost. However, such scaling of MOSFETs has been shown to result in short-channel effects that degrade device performance, particularly as the technology moves into the deep-submicron region, as reported by key players in the industry.\(^1\)

To mitigate this problem, use of high-\(k\) oxide has been introduced.\(^2,3\) High-\(k\) material is proven to result in improved device performance as well as good thermal stability. Despite its success in reducing leakage current, significant reliability issues emerge when using high-\(k\) dielectric, one of which is...
known as negative-bias temperature instability (NBTI). This degradation mechanism has become one of the most prominent limiting factors and is the key reliability issue when scaling complementary metal–oxide–semiconductor (CMOS) technology. NBTI results in a threshold voltage shift for either negative gate voltage or elevated temperature. Nowadays, most of the semiconductor industry\textsuperscript{4–6} has migrated to use of high-\textit{k} dielectrics in integrated circuits, thus increasing concerns regarding the reliability of electronic devices. Therefore, understanding device reliability has become crucial for foundries and integrated device manufacturers to enable better yield and more reliable end-products.

The growing number of publications addressing reliability characteristics of high-\textit{k} dielectrics indicates the increasing interest in this area.\textsuperscript{7–12} However, it appears that most attention has been paid to modeling and measurements of NBTI. Meanwhile, there is still a lack of understanding regarding how the parameters and fabrication processes of high-\textit{k} metal gate stack \textit{p}-channel MOSFETs affect NBTI for deep-sub-nm devices. Understanding the exact mechanism of the hole trap transformation process in each layer of the gate stack is important as this will help researchers to quantify NBTI defect characteristics in order to assess device reliability. Study of the impact of NBTI as a function of design parameters will also help determine security margins during design optimization.

This paper presents a comprehensive simulation study on the effect of geometric and process variables of 32-nm advanced-process high-\textit{k} \textit{p}-MOSFETs on NBTI. Although a few previous works\textsuperscript{13–16} reported on the dependence of NBTI on the gate stack and corresponding processes, none of them further investigated the effects of advanced geometric features such as spacer length or SiGe pocket depth on NBTI. Such advanced geometric features are another new aspect that must be explored, notably in terms of reliability. Considering this requirement, this work focuses particularly on the effects of such advanced geometric features and process parameters on NBTI, as well as identifying the layer in the gate stack which contributes most to NBTI threshold voltage degradation.

**DEVICES AND SIMULATION CONDITIONS**

**32-nm Advanced-Process High-\textit{k} \textit{p}-MOSFET**

The Synopsys TCAD Sentaurus simulator\textsuperscript{17} was adopted to simulate a 32-nm hafnium-based high-\textit{k} dielectric with aluminium nitride (AlN) metal gate \textit{p}-MOSFET, as shown in Fig. 1. The devices used were based on a 32-nm gate-first CMOS process flow, following standard manufacturing trends for such submicron devices. This fabrication process includes shallow trench isolation (STI) formation, high-\textit{k} gate dielectric and metal gate deposition, stress engineering application, as well as use of laser annealing. Implementation of this gate-first CMOS process scheme helps to suppress leakage current, improve drive current, and overcome process-related problems such as ultrashallow junction formation. The laser annealing process was adopted to suppress transient-enhanced dopant diffusion.

Figure 2 compares simulation results for the electrical characteristics with experimental data from Yasutake et al.\textsuperscript{18} obtained on devices fabricated using processes similar to those considered herein. The simulated device shows good agreement with the experimental data, providing confidence that the simulation model is credible.

To study the impact of NBTI for devices with different structures, a wide range of geometric variation was simulated. The geometric parameters that were varied included the thicknesses of the HfO\textsubscript{2} high-\textit{k} layer (2 nm to 4 nm), SiO\textsubscript{2} interfacial layer (0.5 nm to 1 nm), and AlN metal gate (1.8 nm to 6 nm) as well as additional advanced geometrical features including polypitch, spacer length, and SiGe pocket depth.\textsuperscript{13,14,18–22} The effect of a specific design parameter on NBTI was investigated by varying each parameter at a time while keeping the others constant. Regarding the process design, the degradation of the device was studied while varying the boron dose of highly doped drain (HDD), metal gate work function, and halo doping concentration. The geometric structure of the device was fixed in order to study solely the impact of such process variations on NBTI.

**NBTI Simulation Conditions**

The TCAD software adopts a set of physical models including a hydrodynamic transport model and enhanced Lombardi model\textsuperscript{25} with high-\textit{k} degradation where remote Coulomb scattering (RCS) and remote phonon scattering (RPS) are taken into account. The threshold voltage (\(V_{\text{th}}\)) degradation was extracted from the simulation using the on-the-fly (OTF) method\textsuperscript{24} to suppress recovery effects during electrical parameter measurements. Application of prestress voltage is necessary, as it governs the gate bias in setting the initial conditions before the stress stage of the simulation. The NBTI effect was studied at high stress biases with oxide field (\(E_{\text{ox}}\)) of approximately \(-8 \text{ MV/cm} \) to \(-12 \text{ MV/cm} \) and at stress temperatures ranging from room temperature (RT) to 375 K. This work focuses on the properties of as-grown and generated defects, hence stress times from 1 ms to 1000 s were investigated.

**RESULTS AND DISCUSSION**

**Influence of Geometric Variations on NBTI**

The effect on NBTI may be different for different geometric variations. The effect of geometric variations on NBTI was investigated by extensively varying the geometric properties of the thicknesses of the HfO\textsubscript{2} high-\textit{k} layer, SiO\textsubscript{2} interfacial layer (IL),
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Fig. 1. Cross-sectional structure of high-\(k\) gate stack.

![Cross-sectional structure of high-\(k\) gate stack.](image)

and metal gate layer as well as additional advanced features at the 32-nm technology node, including polypitch, spacer length, and SiGe pocket depth.

Figure 2 shows the threshold voltage degradation for different HfO\(_2\), SiO\(_2\), and metal gate thicknesses for stress time of 1 ms, 1 s, and 1000 s and different stress temperatures. It has been reported that, at short stress time, specifically 1 ms, NBTI is dominated by hole trapping at preexisting defects.\(^{28,29}\) The degradation of the threshold voltage, denoted as \(D_{V_{th}}\), is analyzed here. It is apparent from Fig. 3c, f, and i that the preexisting defects are insensitive to temperature and the level of degradation is consistently small for all thicknesses investigated. At stress time of 1 s and beyond, generated defects start to dominate.\(^{28}\) Generated defects are prone to increase at high temperature for high stress time when looking at the difference between room temperature and stress temperature of 375 K for stress time of 1 s compared with 1000 s. However, this difference is distinctly smaller in the metal gate layer. Figure 3 also suggests that the effect of temperature is more significant for smaller than larger thicknesses for stress time of 1 s and 1000 s. This finding is consistent with those of previous studies\(^{30}\) which concluded that, in thinner oxide, the leakage current mechanism is more temperature dependent due to the higher channel surface current caused by either drain-induced barrier lowering (DIBL) or deep channel punch-through currents, which are aggravated at high temperature.\(^{31}\)

The dependence of the threshold voltage degradation on the HfO\(_2\) and metal gate thicknesses indicates higher degradation for greater thicknesses, while SiO\(_2\) contradicts this observation, with thinner SiO\(_2\) seeming to have higher degradation compared with thicker material. Greater HfO\(_2\) thickness in Fig. 3a, and b shows higher \(V_{th}\) shift due to more trapping in the bulk high-\(k\) layer.\(^{32}\) This supports the finding of a considerable amount of defects in the bulk high-\(k\) layer, since the degradation is highly dependent on the thickness of the bulk. On the other hand, a thinner SiO\(_2\) interfacial layer leads to greater \(V_{th}\) degradation, which is in contrast to HfO\(_2\) due to the higher fast transient charging (FTC) effect.\(^{14,32}\) The FTC effect is more important for thinner equivalent oxide thickness (EOT), notably through scaling of the interfacial layer.\(^{33}\) The tunneling barrier for holes in the bulk is also reduced as the SiO\(_2\) IL thickness is reduced, increasing the probability of defect generation or hole trapping in the oxide bulk.\(^{34}\)

Figure 3 also shows that the \(V_{th}\) degradation increases as the metal gate thickness is increased, confirming results in earlier literature\(^{25,35}\) where it was found that increasing the gate thickness enhanced nitrogen diffusion to the silicon interface, consequently increasing degradation. Previously reported chemical analysis by time-of-flight (ToF) secondary-ion mass spectrometry (SIMS) measurements\(^{36}\) to investigate the nitrogen distribution in
the high-κ metal gate stack showed that nitrogen diffuses from metal nitride into the stack during metal nitride and/or poly-Si deposition. Bae et al.\textsuperscript{37} reported that thicker metal gate resulted in higher interface trap density due to stress from the metal nitride layer subsequent to high-temperature annealing. High-temperature annealing causes the agglomeration effect, where crystallites of metal nitride films begin to build up. Growth of such crystallites will result in elastic deformation, eventually introducing stress into the metal nitride layer. Thinner metal nitride layer would lead to lesser diffusion of nitrogen due to nitrogen deficiency, as discussed in Ref. 38. The slope obtained from Fig. 3 shows that changing the SiO₂ IL thickness affects the $V_{\text{th}}$ degradation by 96.16% more than changing the HfO₂ thickness and by 80.67% more than changing the metal gate thickness, for stress temperature of 375 K and stress time of 1000 s. Therefore, it can be summarized that the SiO₂ IL appears to make a prominent contribution to the $V_{\text{th}}$ degradation.

Figure 4 shows the dependence of the oxide field on the thicknesses of the high-κ HfO₂, SiO₂ IL, and metal gate layers for stress time of 1 ms and 1000 s. The $V_{\text{th}}$ degradation is observed to be highly dependent on the oxide field, but this dependence is not affected by the thickness parameters, particularly at lower oxide field. At higher oxide field, the thicknesses of the SiO₂ and metal gate layers seem to influence the threshold voltage shift such that the $V_{\text{th}}$ degradation increases substantially as the SiO₂ thickness is reduced or the metal gate thickness is increased. The oxide field is found to be the cause of creation of interface traps during NBTI degradation of pure oxides,\textsuperscript{39} suggesting that, for the result shown in Fig. 4, more interface traps are created in thinner SiO₂ and thicker metal gate at higher compared with lower oxide field.

The Arrhenius relations for different HfO₂, SiO₂ IL, and metal gate thicknesses are plotted in Fig. 5 to obtain the activation energy ($E_a$). Figure 5 suggests that the activation energy tends to reduce as the thickness is increased, in good agreement with earlier work.\textsuperscript{42} Previous studies\textsuperscript{28,43} found that the overall temperature activation is reduced due to hole trapping. As the gate stack thickness is increased, the hole-trapping volume also increases, leading to lower $E_a$. Figure 6 shows the adjusted $V_{\text{th}}$ shift when the fast and slow traps are separated. One has to subtract the fast trap contribution in order to obtain the slope corresponding to the long-term degradation processes.\textsuperscript{32} The inset shows that the presence of fast traps reduces the time dependence of the overall NBTI. Not much difference in the adjusted $V_{\text{th}}$ degradation can be seen between 2 nm and 3 nm HfO₂ in Fig. 6a. Figure 6b shows the adjusted $V_{\text{th}}$ degradation for two different SiO₂ IL thicknesses. The difference in the $V_{\text{th}}$ shift between 0.5 nm and 0.8 nm SiO₂ seems to be more significant at higher oxide field. A similar observation can be made for the metal gate in Fig. 6c, where the difference in the adjusted $V_{\text{th}}$ degradation is more pronounced at higher than lower oxide field. These results clearly demonstrate that more slow traps/interface traps are generated in thinner SiO₂ and thicker metal gate thickness at higher oxide field, supporting the finding discussed for Fig. 4.
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Additional Advanced Geometrical Features

To further investigate the influence of the geometry on NBTI, additional advanced features including polypitch, spacer length, and SiGe pocket depth were varied. Figure 7 shows the stress temperature dependence for different polypitch, spacer length, and SiGe pocket depth parameters. Smaller polypitch and spacer length resulted in greater sensitivity to temperature, in contrast with SiGe pocket depth, as greater SiGe pocket depth seemed to correspond to greater temperature susceptibility. In literature, it is reported that channel stress is enhanced with polypitch scaling. Scaling the spacer length as well as SiGe pocket depth could also contribute to channel stress. Reducing the spacer length will result in higher channel stress, while reducing the SiGe pocket depth will lead to reduced stress in the channel. Channel stress enhances the hole tunneling probability, thus facilitating breakage of Si–H bonds at the Si–SiO2 interface, which creates more interface traps. Interface traps are sensitive to temperature, the temperature sensitivity is seen in the plots in Fig. 7.

Influence of Process Variations on NBTI

In addition to the geometric parameters, the influence of process design variations on NBTI was also investigated by varying the boron dose of the highly doped drain (HDD), the metal gate work function of the device, and the halo doping concentration.

Boron is widely known to enhance NBTI degradation due to boron penetration into the gate oxide. Boron diffusion from the HDD region into the gate oxide can result in higher initial density of electrically activated defects at Si–SiO2 near channel edges. The threshold voltage degradation over
stress time at 300 K, 350 K, and 375 K for different HDD boron doses is shown in Fig. 8, in agreement with previous study where higher boron dose was observed to cause higher $V_{th}$ degradation.\(^{53}\)

Figure 9 shows the total current density of a device with metal gate work function of 3.0 eV stressed under oxide field of $-12$ MV/cm at stress temperature of 375 K. It is clear that the total current density shows degradation after the device was stressed for 1000 s. The total current density in the channel was reduced by 64.15% after stress. The threshold voltage degradation obtained when varying the metal gate work function is shown in Fig. 10. It is observed that higher metal gate work function resulted in higher $V_{th}$ degradation. The high $V_{th}$ degradation is caused by trapped electrons in HfO$_2$ that discharge to the substrate when the IL is thin, and this problem is aggravated for high metal gate work function, for which more trapped electrons are at energies above the equilibrium Fermi level and are therefore free to discharge to the substrate.\(^{54}\)

Figure 11 shows the $V_{th}$ degradation of a PMOS device with halo doping of $8.5 \times 10^{12}$ cm$^{-3}$ and $5 \times 10^{16}$ cm$^{-3}$ for stress temperature of 400 K for 1000 s. These results reveal no significant change in the threshold voltage degradation when varying the halo doping. This may be due to the halo structure, which is slightly further from the SiO$_2$ bulk interface, where most of the defects are located according to Ref. 55.
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CONCLUSIONS

We present analysis of the effects of geometric and process parameters of advanced-process 32-nm PMOS devices on NBTI. The threshold voltage degradation is observed to increase considerably when the high-k layer or metal gate layer thickness is increased, whereas increasing the SiO₂ interfacial layer thickness results in reduced threshold voltage shift. It is found that the $V_{th}$ degradation shows the strongest dependence on the SiO₂ IL thickness, compared with the HfO₂ high-k or metal gate thickness. Changing the SiO₂ IL thickness is shown to affect the $V_{th}$ degradation by 96.16% more than changing the HfO₂ thickness and by 80.67% more than changing the metal gate, at stress temperature of 375 K for stress time of 1000 s. The temperature insensitivity during short stress time of 1 s indicates absence of generated defects and presence of preexisting defects, as generated defects show strong temperature dependence. At high oxide field, more generated traps are observed for thinner SiO₂ IL and thicker metal gate thickness. This indicates that inclusion of the metal gate after integration of high-k technology can result in substantial BTI effects.

Regarding the process design, higher HDD boron dose is shown to deteriorate the threshold voltage due to penetration of boron into the gate oxide. Our results also show that higher metal gate work function exacerbates trapped carriers in HfO₂, leading to attenuation of the threshold voltage. NBTI is found to be independent of the halo doping concentration, which may be due to the location of the halo structure slightly farther from the SiO₂ bulk interface of the device.

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