Abstract

The paper proposes a technique to demonstrate energy evolution of amorphous oxides defects from the interface depth dispersion using fast ramp laser spike annealing to achieve super activation, in order to significantly assess their impacts on devices with high-k metal gate by numerical analysis. Recovery of trapped charges in HK/MG technologies is intensively studied and provides its capability for highlighting different positively charged defects within and beyond the silicon band gap. The defects vary significantly with energy level as well as in evolution of the $E'$ centers and the interface states densities. The defects in $E'$ centers below Fermi energy level are neutral and unstable, which significantly increase above thermal equilibrium during stressing and driven from valence band to above conduction band energy in fast recovery stage. A correlation of the time dependency for the charged trap concentration, interfacial density and the drain current is observed with current degradation due to the trap accumulation. The analysis shows a strong sensitivity to positive bias activation of the dopant thus been considered for the evaluation of the device
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1. Introduction

The manufacturability of ultra-scaled MOSFETs in the deep-submicron regime with high-k dielectric and metal gate requires a continual target of complicated optimizations between efficiency, reliability and accuracy in order to achieve the performance benchmarks dictated by ITRS [1] and [2]. Such benchmarks require aggressive junction-depth scaling for higher drive current with simultaneous stringent control of short-channel effects (SCE) [3], [4] and [5]. Accurate prediction of lateral dopant distribution and activation has been a persistent concern for the diffusion less annealing [6], [7] and [8], in addition to maximize device performance with fewer defects. The major threat to the reliability of deep submicron CMOS circuits evolved from the positive charge formations within gate dielectric and the generation of permanent degradation of generated interface states [2], [3], [4], [5], [6], [7], [8] and [9]. For pMOSFETs, the negative bias temperature instability (NBTI) is the main concern [10], [11] and [12] and a framework will be proposed for the defects. The three types of positive charges in the dielectric: as-grown hole trapping (AHT), cyclic positive charges (CPC) and anti-neutralization positive charges (ANPC) [11], are illustrated in Fig. 1. Due to this integration of concerns, we investigate the depth dispersion-induced positive charges in high-k/metal gate devices with the substantially improved short-channel performance with higher current capability of fast ramp laser spike annealing to achieve super activation.
We also extensively analyse the impact of strong bias sensitivity variation during discharging process in the switching oxide trap process. We present a comprehensive understanding of types of defects transported in the barrier energies with evolution of the trap states and the threshold voltage degradation due to de-trapping phenomena. The importance of this work signify the depth dispersion not be neglected ($x \neq 0$) as in many previous models, have abandoned the dispersion issue for simplification.

2. Device descriptions and numerical procedure

The samples used in this work are a deep-submicron technology device of 2.3 nm EOT pMOS devices incorporated with advanced-process technology of shallow trench isolation (STI) with intrinsic stress; gate stack consisted of a 0.6 nm SiO$_2$ interfacial oxide layer (IL), and with extensively varied geometry of 2.0 nm thin HfO$_2$ high-k dielectric layer and 5 nm AIN metal gate as shown in Fig. 2. In addition a process procedure
of dipole charge at the high-k oxide interface to investigate the high-k degradation effect has been implemented. After the gate stack deposition, the laser annealing (LA) have been performed in the temperature range from 600 °C to 900 °C to activate the S/D dopants and suppress transient-enhanced diffusion. The laser anneal model used can simulate the inhomogeneous thermal distribution [13], which accurately reflect for stress calculation as well as heat transfer delay in devices. The heat transfer Eq. (1) where $\kappa$, $\rho$ and $C_P$ are the thermal conductivity, mass density and specific heat capacity, respectively. The $\kappa$ and $C_P$ dependent on temperature, in which the measured is taken.

$$\rho C_P \frac{\partial T}{\partial t} = \nabla \cdot (\kappa \nabla T) + G$$

(1)

The heat generation rate $G$ is calculated by Eq. (2) where $I$, $\alpha$ and $d$ represent the light intensity, material absorptivity of light, and depth, respectively, which time and location-dependent.

$$G = I \cdot \alpha \exp \left(-\int_{l=0}^{l=d} \alpha dl \right)$$

(2)

The process temperature, heat boundary conditions during the ramp-up and ramp-down mechanisms, the
light source for the laser pulse and thermal properties of the material are the significant parameters to solve the laser heat annealing equation in (1) and (2). The laser annealing used in this work enhanced the dopant super activation while minimizing significant diffusion, a result that is unattainable by RTA. The wafer was heat up to a high temperature within a very short duration and also allows cooling down quickly by fast heat conduction. Furthermore, the process flow incorporates with advanced stress engineering with epi-SiGe pockets; stress memorization, silicidation, and dual stress liner (DSL) to improve the on-state drain-current drive capability as evidenced by the experimental data in [14].

3. Technique for defects evolution

Several research groups intensively study recovery of trapped charges in HK/MG technologies in the past years and it is difficult to add substantial new insights. The presented data seem to confirm the general consensus. In this submission much more information would be disclosed when a log-time axis would have been used. Distinctions are performed by results carried out in previous works [15] between charged and discharged of oxide defects from the gate-stack with particular experiment set-up developed in Fig. 3. The numerical procedure of the defects distribution was conducted using TCAD Synopsys. The energy probing procedure employs on-the-fly (OTF) method for the measurement in which an initial $I_d-V_g$ is obtained before the sample is exposed to the electrical stress. Fig. 3 demonstrates the procedure of the defects evolution involving energy distribution by has a prior setup of a reference $I_d-V_g$ curve recorded the fresh measurement, $V_g_0$. Then the device was stressed at $V_g = V_g_{st}$ for a pre-specified time. It is shows that $|V_g|$ was then lowered to $|V_{discharge,1}|$. Subsequent to the recording of the drain current as a function of time, the $|V_g|$ is then changed to $|V_{discharge,2}|$ for the next discharging phase and the same procedure applied for different electrical stress. The degradation, $\Delta V_t$, is examined by $V_i$ extraction current level, $I_d = 1.0E^{-7}$ A $\times W/L \mu$m, where $V_{discharge}$ is switched to a constant current sensing level, $V_g_{cc}$. Fig. 4 notes that only a part of an overall degradation during stress is performed within the experimental time window and a large fraction happened prior to the OTF measurement ($t_0 = 1$ ms). The $V_{th}$ degradation monitored at only a certain part by using this technique and as a consequence, the measured threshold voltage shift calculated as $\Delta V_{th} (t_s) = V_{th} (t_s) - V_{th} (t_0)$. Meanwhile, the initial phase of recovery during discharging shows significant logarithmic time dependence and monitored after ($t_0 = 1$ ms) with only the tails of the real recovery curve can be examined experimentally as depicted in Fig. 5.
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Fig. 3.
Defect evolution waveforms involving interface dispersion approaches. After stress, discharging occurs at $V_{\text{discharge}}$, and PCs are periodically monitored by applying a pulse to the gate and recording the drain current at the pulse top through the op-amp, until the discharge completes. The gate bias is then changed to subsequent $V_{\text{discharge}}$ levels for the next discharging phase and the same procedure is applied for the measurement purposes.

Fig. 4.
Hole trapping during charging employs OTF measurement point (1 ms) and determines the $V_{\text{th}}$ shift from the recorded drain current during the discharging phase. The OTF only assesses the change of threshold voltage referred to the first measurement point, and the degradation accumulated before is negligible. Analogously, the NBTI recovery may start already before 1 ms but this
Defects evolution involving interface dispersion approaches in high-$k$/metal-gate deep-submicron CMOS technique can only monitor the tails of the degradation curves.

Fig. 5.
At the initial phase of recovery, logarithmic time dependence is evidently recognizable. However, this behaviour is obscured for relaxation times larger than 1 s where the $\Delta V_{th}(t)$ curve starts to level off as shown in the inset figure. This is anticipated to the fact of the permanent component during NBTI, which is attributed to a hydrogen transition (amphoteric trap) at Pb center, and creates a new interface states controlled by the substrate Fermi level, $E_f$, which thus dominance the trapping rates for hole capture and emission. This is corresponds to the slowly or permanent recoverable component during discharging phase and therefore can be interpreted as the electron occupancy in the defect system.

However, this behaviour is obscured for relaxation times larger than 1 s where the $\Delta V_{th}(t)$ curve starts to level off. This is due to the fact of the permanent component during NBTI and the numerical results fit the experimental charge and discharge curves for a wide range of gate biases able to describe the energy field dependences seen in measurements particularly for the amount of switching traps (PC) stored in the $E'$ center, $\Delta Q_{ox}$ and at the interface states, $\Delta Q_{it}$. The associated switching behaviour is in agreement with the experimental observations made in electrical measurements [16] and [17].

Prior to stress, a reference $I_d$–$V_g$ transfer characteristics was recorded by applying a $V_g$ pulse under $V_{ds} = -50$ mV and $V_{dd} = -1$ V on a fresh device as depicted in Fig. 6. The experiment was conducted on the
2.3 nm HfO$_2$/SiO$_2$ with AlN gate, at stress and measurement temperature of RT. Meanwhile, the $V_g$ corresponding to the last point of each degradation curve in Fig. 7 were extracted in the reference $I_d$–$V_g$ measurement and the $V_{th}$ was measured at a constant current sensing, $I_d = 1.0E^{-7}$ A $\times$ W/L $\mu$m. This is due to the importance of sensed the energy distribution of the positive charges (PCs) at a fixed surface potential. The constant current sensing method used to minimize the uncertainties of a change of surface potential as charging and discharging progresses.

Fig. 6.
Energy evolution by constant current sensing technique. The symbols denote the fresh $I_d$–$V_g$ measurement and the “.” symbol denotes the $\Delta V_{th}$ at 1 ks discharging time at each discharging levels.

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Fig. 7 shows the results of strong discharge bias sensitivity during relaxation. The device was stressed at \( V_{gst} = -2.0 \) V under room temperature, RT for 10 ks. The \( V_{th} \) shift during stress is noted as " .

![Figure 7](image-url)

**Fig. 7**

Results of strong discharge bias sensitivity during relaxation. The device was stressed at \( V_{gst} = -2.0 \) V under room temperature, RT for 10 ks. The \( V_{th} \) shift during stress is noted as " .

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\( \Delta V_{th} \) (V)

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Discharge time (s)

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\( \Delta N_{ox} \) (PCs) and \( \Delta N_{it} \) during discharging measured for 13 different discharging voltages for the thin HK/MG devices with total positive charges considered for the calculation of \( \Delta V_{th} \) demonstrated in Fig. 8. Fig. 8 illustrates the kinetics of the averaged charged traps responsible for the change in occupancy (transition from positively charged center of switching traps to fixed interface charges). An averaged occupation of the charged traps (\( \Delta N_{ox} + \Delta N_{it} \)) results in a faster transition of the charged state and the interface states (\( f_4 \)) require longer time dependency to decay compared to the switching states (\( f_2 \)).
The qualitative degradation and recovery behaviour model predicts a strong sensitivity to positive bias during discharging recovery, which sets in initially at $t_{\text{discharge}} < 10^{-15}$, and after the charge bias switched to the discharging voltages, most defects are positively charged (switching trap state).

Then, a significant number of defects are electrically neutralized in the pico- and nano-second regime by depending on the position of the Fermi-level during recovery. In particular for positive bias, electrons from the conduction band, $E_c$ demonstrated a fast change in occupancy effect (amount of charge visible depending on the Fermi-level) as presented in Fig. 9. The narrow distribution of $\Delta E_B$ were used to distinctly contrast the change in density versus full annealing rather than electrical neutralization. The stress bias switched to recovery voltage, most defects are positively charged, with the discharging accelerated fast when the defects are neutral as confirmed in Fig. 9 and decelerate when most defects are positive. Fig. 10 shows the
evolution of extracting energy distribution for positive charges. During positive recovery, $E_r$ being driven upwards, with the neutralization of $E'$ centers occurred and thereby accelerates the discharging.

Fig. 9.
After the stress bias is switched to recovery voltage, most defects are positively charged, with the discharging accelerated fast when the defects are neutral and decelerate when most defects are positive.
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The evolution of extracting energy distribution for positive charges. During positive recovery, $E_f$ being driven upwards, with the neutralization of $E'$ centers occurred and thereby accelerates the discharging.

Trap density of the defects by activating the depth dispersion ($x \neq 0$), to further converting $V_{\text{discharge}}$ to energy evolution based approach in [15] are depicted in Fig. 11. The positive charge (PC) occupancy effect will manifest a change in the sub threshold, contributing to $\Delta V_{\text{th}}$. This illustrates the importance of monitoring the degradation at applied gate voltage, $V_g$ which mainly dependent on the position of Fermi-level, $E_f$. As for OTF experiments, the Fermi-level is below the valence band edge and most defects will be positively charged [9], [10], [11], [12] and [15]. Meanwhile, during discharging process, the Fermi-level is moved towards band gap and small fraction of the defects will be positively charged and visible as agreed with the experimental results done by our previous work. It is well consensus that positive charges in high-k stacks are dominated below the valence band and within the band gap. As the recovery in our ultra thin oxides with LSA super activation, we conclude that the discovered dispersion in time constants is primarily a property of the Si/SiO$_2$ interface.
4. Conclusions

Excellent results are achieved for positive charges evolution based on the time constants and depth dispersion performances and significantly agreed with the experimental data produced by group [15], supporting the NBTI is resolved of the amorphous interface region. The induced PCs with strong positive bias sensitivity were used to probe both the occupancy effect as well as the impact of the occupancy on the degradation and recovery dynamics, being particularly significant for drain current change in the threshold voltage improvement.

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