Active damping network in DC distributed power system driven by photovoltaic system

Awang Jusoh a, Hani Baamodi a,*, Saad Mekhilef b

a Department of Energy Conversion, Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81300 Johor, Malaysia
b Department Of Electrical Engineering, Faculty of Engineering Building, University of Malaya, 50603 Kuala Lumpur, Malaysia

Received 21 June 2012; received in revised form 22 September 2012; accepted 29 September 2012
Available online 13 December 2012

Abstract

An instability phenomenon may occur in DC electrical systems due to undesirable source–load interaction and the behavior of power electronic loads that act as a constant power load. The present study focuses on DC electrical systems associated with constant power behavior. The phenomenon occurs such that each converter has its own internal control function for its output voltage regulation. The converter tends to draw a constant power which therefore produces negative incremental input impedance within its bandwidth. An active damping technique is proposed to improve the stability of a DC electrical system consisted of photovoltaic arrays, an LC filter and a constant power load. The active damping network was controlled to behave as a small-signal effective damping resistor over a DC network so that any instability in the DC bus will be reduced and eliminated. This technique eliminates the oscillations produced by the constant power load. MATLAB/SIMULINK modeling and simulation are used to confirm the validity of the proposed technique.

Keywords: Active damping network; Distributed power system; DC bus instability phenomenon; Constant power load; Photovoltaic arrays

1. Introduction

Commonly, there are two types of loads in the electrical systems, namely; the conventional positive resistive load that requires constant voltage for its operation and the constant power load (CPL) that consumes a fixed amount of power regardless of the received voltage (Rivetta et al., 2005). A CPL is a power electronic converter that sinks a constant power from the system bus and produces a constant power characteristic in which the supply voltage reduces when the input current increases. This subsequently leads to an incremental of negative impedance (Cespedes et al., 2010).

The behavior of constant power load becomes a concern for DC distributed power systems (DPS) such as those found on More Electric Aircraft (MEA) and electric vehicles. The increasing use of CPL will result in complex DPS with multiple power electronic converters to supply various static and dynamic loads (Emadi et al., 2006). However along with many benefits associated with DPS, such as reduction in overall system weight, cost, and maintenance, it may present several problems. One possible problem might be a loss of system stability in the DC bus bar due to the undesirable source–load interaction and the negative incremental resistance produced by constant power loads (Cespedes et al., 2010; Xinyun et al., 2007). The analysis of DPS becomes more complicated due to system complexity and involvement of different types of load converters that act as constant power loads. Nevertheless, the study and analysis of these systems become easier if one considers only a single load converter that has been
supplied by any primary source such as Photovoltaic system.

As energy demands around the world increase, the need for renewable energy sources that will not pollute the environment has been increased (Moradi and Reisi, 2011). Solar energy is one of the renewable sources that depends on weather factors, essentially the irradiation (Teng-Fa et al., 2009). The photovoltaic system is practically suited for distributed resource applications and has now emerged as an established commercial technology with a number of major manufacturers producing the equipment (Chin et al., 2011). However, as it is a renewable source, care is required if the diffuse and variable energy resource is to be converted into electricity at a reasonable cost. The photovoltaic (PV) System is the most promising as a source of future electricity generation (Wang, 2006). The main problem of the PV system is that natural irradiation causes voltage and power fluctuation problems at the load side (Uzunoglu et al., 2009). In addition to that the power available from PV source is difficult to be completely captured. For PV, the maximum power is depending on the voltage under different conditions (i.e. temperature and irradiance) (Moradi and Reisi, 2011; Saloux et al., 2011).

One of the techniques utilized to compensate the instability problem associated by CPL and PV power fluctuation is by using passive damping in which a resistance and high value of capacitance are used. However, this technique will result in a large amount of power dissipation and the passive components can be bulky (Rahimi and Emadi, 2009a; Yushan et al., 2012). Another technique for compensating is the use of active damping. Active damping is generally a network that draws or returns current to the DC bus in order to damp any instability (Jusoh, 2004a; Xinyun et al., 2007). The active damping network is a bidirectional DC–DC converter in which its control loop forces it to draw an input current that is proportional to the DC bus voltage to present positive impedance to the supply. This positive impedance plays an important role in compensating the negative impedance represented by CPL and thus ensuring the system stability (Jusoh, 2004b).

In this paper, the implementation of active damping network is presented. The proposed active damping is intended to stabilize the system that consists of photovoltaic arrays (PVA), an LC filter and CPL. This paper has been organized as follows. The modeling of solar photovoltaic cell/module is discussed in Section 2. In Section 3, constant power load and its negative incremental resistance are reviewed. Section 4 describes the application of the active damping method to the DC bus of the photovoltaic system. It is clearly shown that the DC bus system that supplies the CPL can be stabilized effectively using this method. Simulation results to prove the effectiveness of the proposed method are presented in Section 5, and finally, the conclusions are drawn in Section 6.

2. Solar photovoltaic system

The photovoltaic system directly converts sunlight into electricity that can be used for multiple-purposes. In this paper, a large PV system consists of a set of PV cells connected in series and parallel to produce the power required by the DPS source in a system that consists of constant power load. Fig. 1 shows the typical equivalent circuit representing a PV cell (Chin et al., 2011; Yuncong et al., 2011). This circuit contains a photo current source $I_{ph}$, a diode $D_1$, series, $R_s$ and parallel $R_p$ resistors (Saloux et al., 2011).
The well-known diode equation stated in Eq. (1) is appropriate in describing the operation of p–n junction solar PV cell (Jensen et al., 2010; Pandiarajan and Muthu, 2011). The output current can be derived as a function of the output voltage of this cell that is:

$$I = I_{sc} - I_s\left(e^{V/R_s} - 1\right) - \frac{(V + IR_s)}{R_p}$$  \hspace{1cm} (1)

where $I$ and $V$ are the output currents and voltage produced by photovoltaic. A number of solar modules are connected in a series to form a required higher voltage. In this application, 12 modules are connected in a series to produce a total output voltage of 270 V. The solar PV can be modeled using MATLAB/SIMULINK based on Eq. (1). Fig. 2 shows the single photovoltaic mathematical model represented by a subsystem with insolation and feedback current as inputs, power and voltage as outputs (Altas and Sharaf, 2007).

2.1. Maximum power point tracking (MPPT)

Since the power produced by solar PV depends on the operation and surrounding conditions, it is essential to implement a maximum power point tracking (MPPT). The type of MPPT algorithm used in this paper is perturb and observe (Boico and Lehman, 2012). This type employs a simple feedback arrangement and few measured parameters. In this approach, the array current is periodically given a perturbation and the corresponding output power is compared with that at the previous perturbing cycle (Houssamo et al., 2010; Moradi and Reisi, 2011; Yuncong and Abu Qahouq, 2011). The nonlinear nature of a PV cell affects the DC bus voltage since the output current and power of the PV cell depends on the temperature and irradiance (Yu et al., 2004). With an increase of working temperature, the short-circuit current of the PV cell increases whereas the open-circuit voltage and the maximum output power decreases (Houssamo et al., 2010; Uzunoglu et al., 2009). MPPT method is applied to obtain a maximum power tracking and this leads to some changes in the bus voltage. The main objective of MPPT is to adjust $I = I_{ref}$ where $I_{ref}$ is the required current so that PV generates maximum power point (MPP) at all conditions. Fig. 3 shows the flowchart of producing the maximum power point.

The MPPT algorithm shown in Fig. 3 is used to achieve the maximum power point of PV that is used as a source to run the constant power load with and without using the active damping circuit which will be discussed in detail in Section 4 in order to examine the DC bus instability.

3. Constant power load

Usually, when DC/DC converter drives another DC/DC converter, it regulates output voltage tightly to ensure a power quality requirement. If the output voltage of the source converter increases for some reason, the load converter will reduce the duty ratio to regulate the output voltage which will reduce load current and vice versa. Therefore, the source converter sees load as a constant power load (Seyoung and Williamson, 2011).

3.1. Negative incremental resistance of CPL

When the load converter tightly regulates its output, it tends to behave like a constant power load which has a negative incremental impedance characteristic (Rahimi and Emadi, 2009b; Rivetta et al., 2005). Examples of CPL devices are DC/DC converters and DC/AC inverters.
Each converter has its own internal controller to regulate the output voltage or to control the speed of a motor. Because of this, it will tend to draw constant power and produce constant power characteristic (Emadi et al., 2006). If there is any voltage disturbance occurring at the DC source side, the converter will try to maintain the constant power required by the load. Due to the constant power characteristic (of average inductor current and average capacitor voltage behavior of the switching converters. From Fig. 6, the rate of average inductor current and average capacitor voltage are developed as expressed in the following equations.

\[
\frac{dI_m}{dt} = \frac{V_L}{L} \quad \text{or} \quad I_m = \frac{V_L}{L}
\]

And

\[
\frac{dV_c}{dt} = \frac{I_m}{C} \quad \text{or} \quad V_c = \frac{I_m}{C}
\]

The average value of the inductor voltage is given by

\[
V_L = \frac{1}{T} (I_m D T - (V_0 - I_m)(1 - D))
\]

\[
= V_m D - (V_0 - V_m)(1 - D) = V_m - V_0(1 - D)
\]

Therefore,

\[
I_m = \frac{V_m - V_0(1 - D)}{L}
\]

Similarly the average capacitor voltage is given by

\[
V_c = \frac{I_m}{C}
\]

The average state space model of the converter

The average state space approach is most widely used in the power electronics field in order to study the dynamic behavior of the switching converters. From Fig. 6, the rate of average inductor current and average capacitor voltage are developed as expressed in the following equations.

4. Active damping circuit

Active damping is generally a network that draws or returns current to the DC bus in order to damp any instability. An active damping circuit is a bi-directional DC–DC converter which may be used to perform an active damping function in a distributed power system (DPS) comprising photovoltaic arrays, an L–C filter and constant power load (CPL). Fig. 6 shows the active damping circuit with its control loops.

From Fig. 6, the transistors T1 and T2 are operated in anti-phase with variable duty cycle. The duty cycle of T2 is D. The converter will operate in two modes depending upon the direction of the converter inductor current, I_m and the direction of the energy flow in the converter. When I_m is positive, the circuit operates like a boost converter to step up its output voltage, the current is switched between T2 and D1 and energy is delivered to the capacitor. When I_m is negative, the circuit operates as a buck converter to step down its output voltage, taking energy from the capacitor, C and returning it to the DC bus. Devices T1 and D2 are then carrying the inductor current. There will be no energy transfer between the converter and the DC bus as presented in (Jusoh, 2004a). In order to analyze the system, a set of fixed parameters are chosen as in Table 1 below.

The value of inductance is chosen in such a way as to achieve a small overshoot and the value of capacitance is set to be high in order to have sufficient energy storage and to reduce the output ripple. To simplify the simulation process, an averaged converter model for the bi-directional DC–DC converter is developed.

4.1. The average state space model of the converter

The average state space approach is most widely used in the power electronics field in order to study the dynamic behavior of the switching converters. From Fig. 6, the rate of average inductor current and average capacitor voltage are developed as expressed in the following equations.

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And

\[
\frac{dV_c}{dt} = \frac{I_m}{C} \quad \text{or} \quad V_c = \frac{I_m}{C}
\]

The average value of the inductor voltage is given by

\[
V_L = \frac{1}{T} (I_m D T - (V_0 - I_m)(1 - D))
\]

\[
= V_m D - (V_0 - V_m)(1 - D) = V_m - V_0(1 - D)
\]

Therefore,

\[
I_m = \frac{V_m - V_0(1 - D)}{L}
\]

Similarly the average capacitor voltage is given by

Fig. 4. (a) Negative resistance behavior of CPL. (b) Module of CPL.

Fig. 5. Model of source connected to CPL via L–C filter.
\[
T_c = \frac{1}{T} (T_{in} (1 - D)) T = T_{in} (i - D)
\]  
(8)

Therefore,
\[
\bar{V}_a = \frac{T_{in} (1 - D)}{C}
\]  
(9)

Fig. 7 shows the average model that represented the active circuit according to Eqs. (7) and (9) of inductor current and capacitor voltage respectively.

Eqs. (7) and (9) contain products of the circuit variables and the transistor duty-ratio, therefore they must be linearized. Taking a first order approximation for the Taylor series of the variables gives Eqs. (10) and (11):

\[
\frac{\delta I_{in}}{C_{15}} = \frac{1}{L} \frac{\delta V_{in}}{C_0} (1 - D) T_{in} + \frac{\bar{V}_o \delta D}{L}
\]  
(10)

\[
\frac{\delta \bar{V}_o}{C_{15}} = \frac{(1 - D)}{C} \delta T_{in} - \frac{T_{in} \delta D}{C}
\]  
(11)

Eqs. (10) and (11) are two simultaneous equations, with two independent variables \(\delta T_{in}\) and \(\delta \bar{V}_o\), and two inputs \(\delta V_{in}\) and \(\delta D\). In order to obtain transfer function relations, these two equations are converted to the Laplace domains, Eqs. (12) and (13):

\[
\frac{\delta I_{in}}{C_{15}} = \frac{1}{L} \frac{\delta V_{in}}{C_0} (1 - D) T_{in} + \frac{\bar{V}_o \delta D}{L}
\]  
(12)

\[
\frac{\delta \bar{V}_o}{C_{15}} = \frac{(1 - D)}{C} \delta T_{in} - \frac{T_{in} \delta D}{C}
\]  
(13)

Substituting Eq. (13) into Eq. (12) so that the \(\delta \bar{V}_o\) can be eliminated and the small-signal inductor current can be represented in terms of the small-signal input voltage and small-signal duty ratio.
In order to obtain the transfer function between small-signal input current and small-signal duty ratio, the small change in the input voltage, $dV_m$ can be neglected. This is possible since these are linear equations. The small-signal transfer function between duty-ratio and the converter input current of the DC–DC converter is shown in Eq. (15).

$$\frac{dI_m}{dD} = \frac{sI_{in} + T_m(1-D)}{sCL^2}$$  

Eq. (15) indicates that the system poles depend upon the steady-state duty-ratio, but are always located on the imaginary axis of the complex $s$-plane, which indicates that the system stability is in a critical condition.

4.2. Control loops

The capacitor voltage and inductor current of the DC/DC converter are used as feedback signals. Any oscillation caused by input disturbance and step-changing load conditions have to be compensated by forcing the DC/DC converter to switch its operating mode to boost converter mode or buck converter mode depending on the reference current $I_{inref}$.

4.2.1. Current control loop

In order to force the converter input current to follow a command signal, a feedback loop is added around the system as shown in Fig. 8. $I_{in}$ is compared with the command or reference signal $I_{inref}$, the error is then passed through an integral controller having a compensator zero and gain $K_a$ to form the duty ratio for the converter.

Using Eq. (15), the open loop transfer function of the system in Fig. 8 is given by

$$\frac{\delta I_{m}}{\delta I_{inref}} = \frac{s \frac{T_m}{L} + \frac{T_m(1-D)}{CL}}{s^2 + \frac{(1-D)^2}{CL^2}} K_a$$

From Fig. 8, it is found that the closed loop transfer function of the current control is as stated in Eq. (17):

$$\frac{\delta T_m}{\delta I_{inref}} = \frac{s \frac{T_m}{L} + \frac{T_m(1-D)}{CL}}{s^2 + \frac{(1-D)^2}{CL}} K_a$$

Fig. 8 shows the plot of root locus of the system poles of Eq. (18) as the control gain $K_a$ varies from zero to infinity for two positive values of $I_{in}$. The following parameters are used in all the plots: $z = 1000$ rad/s$^{-1}$; $L = 1$ mH, $C = 1$ mF, $V_o = 400$ V, $I_{in} = \pm 3$ A and $\pm 30$ A; $D = 0.325$. The plot in Fig. 9 shows that there are three poles and two zeros in the system. The poles have same movement patterns with different current levels. The complex poles begin at the imaginary axis and move to the left-hand side of the $s$-plane, one towards the zero and the other towards minus infinity on the real axis. The pole at the origin moves with different directions, depending upon the current. For the positive current, it moves to the left towards the zero, moving further to the left with higher currents.

The choice of the zero position is to control the transient response of the system. For a small zero value, the system closed loop poles are positioned near to the origin, which results in slow dynamics in the system. Too high a value for the zero results in the complex pole locus remaining close to the imaginary axis and a very high value of $K_a$ is required to move the poles well into the left-half plane. An intermediate value for the zero is therefore most desirable.

The bandwidth of control loop is chosen to be 4.5 kHz (28 krads$^{-1}$) to obtain a unity gain frequency of the loop. For the design requirement, the switching frequency should be four times larger than the bandwidth in order to prevent switching related instabilities in the control loop. Therefore, the switching frequency selected is 20 kHz. In order to obtain a bandwidth of 28 krads$^{-1}$ as discussed in (Jusoh, 2004a), a zero compensator must be chosen to be at least one decade below the cross-over frequency that is

![Fig. 8. Closed loop system of current control.](image-url)
z = 1000 rads\(^{-1}\) and the forward gain \(K_a\) must be chosen to be 0.07 that is:

\[
K_a = \frac{\omega_{oa} * L}{V_0} = \frac{28K * 1 \text{ mH}}{400} = 0.07
\]

4.2.2. Voltage control loop

DC–DC converter requires a voltage loop to ensure that the converter output voltage returns to its nominal value after any disturbance or any transience happens. Fig. 10 shows the block diagram of current and voltage control loops.

The closed loop transfer function in Eq. (17) is approximately unity from low frequency up to its cross-over frequency \(\omega_{co}\). That is \(\frac{I_{ref}}{I_{in}} = 1\). Therefore, the transfer function of Fig. 10 is given by:

\[
\frac{V_0}{I_{in}} = \frac{V_c}{I_{in}} = \frac{V_c}{I_{in}} \times \frac{I_{in}}{I_{inref}} = \frac{1}{sC} \times (1 - D) \times 1
\]

At the cross over frequency, the magnitude of the loop transfer function should be unity as in (Jusoh, 2004a), that is \(1 = \frac{I_{out}}{I_{in}} = \frac{1}{1 - sD} \times \frac{1 - D}{1 - sD} \times K_c\). This equation indicates that the cross over frequency of the voltage control loop is proportional to the voltage controller gain for a fixed value of \(D\).

Voltage controller loop bandwidth \(\omega_{vo}\) must be chosen to be much smaller than \(\omega_{oa}\) in order to ensure that the voltage control loop does not interfere with the current loop. Therefore, \(\omega_{oa}\) is chosen to be 3 rads\(^{-1}\). Assuming \(C = 200 \mu\text{F}\) and \(D = 0.5\), \(K_v\) is calculated to be 0.0012.

4.2.3. Complete active damping circuit

The current reference signal, \(I_{ref}\) for the high bandwidth current control loop is derived from DC bus voltage \(V_{in}\) through the transfer function \(h_r(s)\) which is effectively a DC-blocking high pass filter. The transfer function \(h_r(s)\) that provides the input current reference as shown in Fig. 6 is a high pass filter having a high frequency gain, \(K_r\), given by Eq. (21).

\[
h_r(s) = \frac{I_{in}}{V_{in}} = \frac{sK_r}{s + \omega_f}
\]

The impedance becomes constant as the frequency passes the high pass filter corner frequency, \(\omega_f\).

\[
I_{in} = \frac{1}{1 + \frac{1}{\omega_{co}}} = \frac{\omega_{co}}{s + \omega_{co}}
\]

So, \(V_{in} = \frac{(s + \omega_{co})(s + \omega_f)}{K_r \omega_{co} s} = Z_D\)

The corner frequency, \(\omega_f\) and the gain \(K_r\) of the reference transfer function were chosen to be constant at 1000 rads\(^{-1}\) and \(K_r = 2\) to ensure that the damping system input impedance is resistive in the region of the filter natural frequency and to provide a well-damped transient response. Fig. 11 shows a complete active damping network.

5. Simulation results

MATLAB/SIMULINK simulations have been performed to examine the effect of CPL to the DC bus instability when driving by PV arrays (PVA). A simulation of the DC system is done with and without active damping to show the validity of active damping in reducing the system instability. The SIMULINK model of Fig. 12 has been
simulated to examine the instability of the DC system. A 5 kW constant power load is applied to the system that consists of a PVA of 270 V through an L–C filter with a small value of resistance in the series with the inductance to ease the simulation and to represent the winding resistance, where $L = 150 \mu\text{H}$, $C = 300 \mu\text{H}$ and $R = 0.15 \Omega$.

### 5.1. Simulation of CPL and PVA without active damper

Fig. 12 is a simulation circuit in which the active damper is removed. Figs. 13a and 13b show the simulated capacitor voltage and inductor current respectively when +10 V transient occurred in the PVA source voltage at simulation time.
of 3 s for a period of 0.04 s and then steps back to its nominal value at 3.04 s. Also, a $-10 \text{ V}$ transient occurred in the PVA source voltage at simulation time of 3.06 s for a period of 0.04 s and then steps back to its nominal value at 3.1 s. The DC voltage abruptly steps from 270 V to 280 V for a positive transient and from 270 V to 260 V for a negative transient.

The simulation waveforms show oscillations occurring in the capacitor voltage and inductor current when there is a transient voltage applied to the DC bus. The oscillation is due to the behavior of CPL. CPL has a negative incremental resistance that causes a loss of system stability in the DC bus under transient conditions. Voltage at the DC bus is increased and oscillates before it returns to its nominal value. There is a small voltage drop in the DC bus voltage due to the use of small series resistance. The oscillation in the capacitor voltage and inductor current is increased when a higher power level of the constant power load is applied. Figs. 14a and 14b show the simulated capacitor voltage and inductor current respectively for the same step voltages for different power load levels which are 5 kW and 10 kW.

Figs. 14a and 14b show clearly that capacitor voltage and inductor current for 10 kW is more unstable compared with 5 kW. At higher power levels, the small-signal resistance of the CPL has a lower magnitude under this condition compared to system resistance.

5.2. Simulation of CPL and PVA with active damper

Fig. 12 is again simulated where the averaged model of DC–DC converter is used with 5 kW CPL driving by PVA system. The control system parameters are $K_r = 2 \Omega^{-1}$, $\omega_{co} = 28 \text{ krads}^{-1}$, $\omega_f = 1000 \text{ rads}^{-1}$, $\omega_{vo} = 3 \text{ rads}^{-1}$, $L_s = 150 \mu\text{H}$ and $C_s = 300 \mu\text{F}$ and $V_0 = 400 \text{ V}$. The circuit is simulated with the same conditions as stated in Section 5.1, where there is a positive and negative transient occurred in the DC bus at simulation time of 3 s for positive and at 3.06 s for negative transient with a period of 0.04 s. Figs. 15a and 15b show the simulated capacitor voltage and inductor current in which the system is well damped. The oscillation found in Section 5.1 has been removed. The use of active damping plays an important role in system stability and it avoids system failures. This is because the impedance represented by the active damping compensates the negative impedance produced by CPL.

Figs. 16a and 16b show the converter output voltage and current respectively in which the positive transient changes in the DC bus voltage result in a flow of energy represented by positive $I_{in}$ into the active damping circuit and an associated increase in the capacitor voltage of the active damping $V_O$, whilst the negative transient in the DC bus voltage results in a discharge of the capacitor. The output voltage will return to its nominal value due to the voltage control loop.
Fig. 14a. Simulation waveform of capacitor voltage, $V_c$ for 5 kW and 10 kW.

Fig. 14b. Simulation waveform of inductor current, $I_L$ for 5 kW and 10 kW.

Fig. 15a. Simulation waveform of $V_{in}$ for a ±10 V transient in the DC bus voltage.

Fig. 15b. Simulation waveform of $I_{in}$ for a ±10 V transient in the DC bus voltage.
5.3. Simulation of multiple CPLs and PVA without active damper

The simulation for a single CPL is repeated with multiple CPLs. Fig. 17 has been simulated in which the damping circuit is removed in order to examine the instability of the DC system when multiple CPLs are applied. The total connected power load is 16 kW comprising of 1 kW, 5 kW and 10 kW.

Figs. 18a and 18b show the simulated capacitor voltage and inductor current respectively when ±10 transient occurred in the DC bus voltage.
Fig. 18a. Simulation waveform of $V_{in}$ for a $\pm10$ V transient in the DC bus voltage.

Fig. 18b. Simulation waveform of $I_L$ or a $\pm10$ V transient in the DC bus voltage.

Fig. 19a. Simulation waveform of $V_{in}$ for a $\pm10$ V transient in the DC bus voltage.

Fig. 19b. Simulation waveform of $I_L$ for a $\pm10$ V transient in the DC bus voltage.
The waveforms above show that the system experiences an oscillation because of the negative equivalent resistance produced by the load. This is due to the non-linear characteristic among the parallel CPLs, which leads to instability phenomenon in the system. Thus, the active damping circuit needs to be applied to the DC bus in order to compensate for the oscillation.

5.4. Simulation of multiple CPLs and PVA with active damper

Fig. 17 is again simulated where the averaged model of DC–DC converter is used with multiple CPLs being driven by the PVA system. The circuit is simulated with the same conditions as stated in Section 5.3 where there is a positive and negative transient occurring in the DC bus at simulation time of 3 s for a positive and at 3.06 s for a negative transient with a period of 0.04 s. Figs. 19a and 19b show the simulated capacitor voltage and inductor current in which the system is well damped.

Figures above satisfy the use of active damping in DPS resulting in reduction of the oscillation. The system becomes more stable and reliable for high power applications.

6. Conclusion

One possible problem with DPS might be a loss of system stability in the DC bus bar due to an undesirable source–load interaction and the negative incremental resistance produced by constant power loads. The active damping circuit was proposed to improve the stability of a DC electrical system consisted of photovoltaic arrays, an LC filter and a constant power load. The averaged model of the bi-directional of DC–DC converter was introduced to act as an active damping. It has been controlled to behave as small-signal effective damping resistor across the DC network. Therefore, it can reduce the instability at the DC bus bar at transient in DC bus voltages and it is reliable for high power levels. The instability phenomenon was examined and the operation of active damping network in reducing the oscillation was confirmed by using MATLAB/SIMULINK.

Acknowledgement

The authors wish to acknowledge the Universiti Teknologi Malaysia (UTM) for financial support under Research University Grant (Vot. Q.J130000.2623.02J46).

References

Further reading
