Voltage vector control of a hybrid three-stage 18-level inverter by vector decomposition

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Abstract: This study presents a three-stage 18-level inverter design and its innovative control method. The inverter consists of a series-connected main high-, medium- and low-voltage stages. The high-voltage stage is made of a three-phase, six-switch inverter. The medium- and low-voltage stages are made of three-level inverters constructed by H-bridge units. The proposed control strategy assumes a reference input voltage vector and aims to operate the inverter in one state per sampling time to produce the nearest vector to that reference. The controller operates to reach the desired state with minimum switching actions, giving the priority in switching reduction to the higher voltage stage. The approach of the proposed control strategy has been presented, a set of related terms has been defined and the implementation process has been described. The test results verify the effectiveness of the proposed strategy and the capability of the inverter to produce low-voltage distortion and switching losses.

1 Introduction

Multilevel inverter (MLI) refers to the class of inverters with output points, which have more than two voltage levels with respect to the negative terminal of the input supply [1]. The essential virtue of MLIs over the conventional inverters is the capacity to have output voltage and current levels higher than those of the device ratings; hence, MLIs have been classified as high-power inverters [2]. Increasing the number of levels improves MLI characteristics by reducing harmonic distortion both at input and at output sides, $\frac{dv}{dt}$ stress, and switching losses [3]. These advantages do not come free or cheap; MLI circuits are more complicated than the basic inverter circuit, apply more components and are more expensive to implement. Despite that, recent studies recommended MLI topologies for medium-voltage applications [4].

1.1 Hybrid MLI topologies

The basic MLI circuits have equal or equally divided input dc voltages, and the number of levels is linearly related to the number of switching devices. The maximum number of levels achievable with basic MLI topologies is limited because of cost and size considerations. Increasing the number of levels is a temptation, as it enhances the MLI merits.

The approach of asymmetrical MLI based on supplying the inverter with unequal input voltages is found to have the capability of producing a higher number of levels for the same number of components compared to the basic MLI [5].

The MLI design can be further optimised by hybridisation, that is to create an MLI by cascading smaller dissimilar inverter circuits [3]. According to the hybridisation level this has been done as follows:

1. Cascading H-bridge cells consist of different types of switching devices that operate at different voltage levels and frequency [6]. The switch characterised by low conducting losses is used for the high-voltage stage, and the fast switch is applied for the high-frequency stage.

2. Constructing the inverter with cascaded stages of different topologies, for example, H-bridge three-level stage(s) in series with neutral point clamped (NPC) three-level stage [7, 8] or to the six-switch two-level stage [9]. Better tradeoff between the cost and number of levels has been achieved.
3. In [10], a linear mode amplifier has been added in series to eliminate the need for PWM switching; this design has not gained popularity despite the claim of providing higher efficiency compared to other designs.

### 1.2 Control of MLI

Many studies have reported the control of the MLI. The initial studies have used the multiscarrier PWM strategy. The space vector modulation (SVM) control has been introduced and implemented [11–13]. The carrier-based SVM has been developed for MLIs with any number of levels [14].

Fundamental frequency switching with selected harmonic elimination has been implemented exploiting the high number of levels provided by asymmetric MLI to reduce the switching losses [15]. This method however requires a pre-calculated switching angles lookup table. In [16], fundamental-frequency SVM has been applied utilising the high number of levels provided by the four-stage asymmetrical inverter.

### 1.3 Scope of the paper

A hybrid MLI of cascaded stages of two- and three-level inverters is presented in this paper. The inverter circuit is given in the following section. The controller receives the input of sampled reference voltage vector. The control concept is based on the hypothesis that with sufficiently high number of levels, the typical SVM approach of combining three states to achieve the reference voltage can be abandoned. Instead, the reference vector is approximated to the nearest inverter’s vector. The control strategy is introduced in Section 3. Implementation is described in Section 4. In Section 5, selected test results of the developed inverter and strategy are demonstrated.

### 2 Inverter topology, voltage vectors and switching states

One of the basic MLI topologies is the cascaded H-bridge cells. This topology has the advantage of modular structure where the inverter consists of small identical cells. The main drawback of this topology is the requirement for high number of isolated dc sources. The k-cell per arm inverter has \(2k + 1\) levels and requires \(3k\) isolated dc sources.

The number of levels has been greatly increased with asymmetrical sourcing [15]. The asymmetry resultant by supplying various stages with different dc voltage levels results in a voltage step of each cell different from other cells in the same inverter arm. It has been reported in many studies that the maximum number of uniform steps is achieved when the dc voltages of the arm cells form a ratio-3 geometric sequence. Study of the appropriate voltage ratio shows that the modulation condition required to avoid high-frequency operation at high-voltage stage is satisfied if any two adjacent voltage levels can be achieved by switching the lowest voltage cells only [17]. This condition cannot be satisfied with ratio-3 dc sources, and hence this selection is not appropriate for PWM control. Yet this ratio has been followed by some designs that do not apply PWM control [15, 16].

This paper deals with the two main drawbacks of the cascaded H-bridge MLI, which are the requirement of a large number of isolated dc supplies and the possible high switching frequency of the high-voltage stage. The presented circuit saves the cost of the dc supplies by reducing the number of the high-voltage stage sources to one. The avoidance of high switching frequency at the high-voltage stage is ensured by the suggested control strategy.

The inverter circuit shown in Fig. 1 consists of the ‘main’ high-voltage six-switch inverter, with each output line connected in series to two cascaded single-phase full bridge inverters. The main and H-bridge cells are fed by isolated dc sources of \(9V_s\), \(3V_s\), and \(V_s\) as shown. This voltage ratio provides an 18-level inverter. In this design, the high-voltage stage has only one dc source operating with reduced current ripple compared to the three dc sources of the cascaded H-bridge design [15, 16]. Therefore considerable saving in the dc source cost and losses can be achieved with this arrangement.

Although the conventional MLI design aims to divide the input voltage equally between the switching devices, hybrid MLI design depends on the essential feature of semiconductor switching devices technology, which implies a tradeoff in device selection in terms of switching frequency and voltage-sustaining capability [3, 6, 8, 9, 15]. The inverter of Fig. 1 is no exception, where the main inverter switch is essentially subjected to \(9/13\) of the total dc voltage; however, this stage operates at the output voltage fundamental frequency and slow switching devices such as GTO can be employed if the inverter is to be constructed with high-voltage ratings.

### 2.1 Voltage vectors and inverter states

The switching variables of the inverter are denoted by \((x_{ab}, y_{ab}, z_{ab})\), where \(x\) is a binary digit whereas \(y\) and \(z\) are trinary digits. The states of the high-, medium- and low-voltage stages are determined by \(x_{ab}, y_{ab}\) and \(z_{ab}\), respectively. The output voltage vector can be represented in terms of the switching state as shown in the following derivation.

Line voltages are represented in terms of the switching variables in (1)

\[
\begin{align*}
\begin{bmatrix}
  v_{ab} \\
  v_{bc} \\
  v_{ca}
\end{bmatrix} = 9V_s \begin{bmatrix}
  x_a - x_b \\
  x_b - x_c \\
  x_c - x_a
\end{bmatrix} + 3V_s \begin{bmatrix}
  y_a - y_b \\
  y_b - y_c \\
  y_c - y_a
\end{bmatrix} \\
+ V_s \begin{bmatrix}
  z_a - z_b \\
  z_b - z_c \\
  z_c - z_a
\end{bmatrix}
\end{align*}
\]
Phase voltages of the Y-connected load can be represented as follows:

\[
\begin{bmatrix}
  v_{an} \\
  v_{bn} \\
  v_{cn}
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
  v_{ab} - v_{ca} \\
  v_{bc} - v_{ab} \\
  v_{ca} - v_{bc}
\end{bmatrix}
\]

\[
= \frac{V_s}{3} \begin{bmatrix}
  2 & -1 & -1 \\
  -1 & 2 & -1 \\
  -1 & -1 & 2
\end{bmatrix} \begin{bmatrix}
  9x_a + 3y_a + z_a \\
  9x_b + 3y_b + z_b \\
  9x_c + 3y_c + z_c
\end{bmatrix}
\]

The voltage vector is achieved by Park’s transformation given in (3):

\[
\begin{bmatrix}
  v_D \\
  v_Q
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
  0 & -0.5 & -0.5 \\
  \sqrt{3} & -\sqrt{3} & 0
\end{bmatrix} \begin{bmatrix}
  v_{am} \\
  v_{bm} \\
  v_{cm}
\end{bmatrix}
\]

\[
= \frac{V_s}{3} \begin{bmatrix}
  1 & -0.5 & -0.5 \\
  \sqrt{3} & -\sqrt{3} & 0
\end{bmatrix} \begin{bmatrix}
  9x_a + 3y_a + z_a \\
  9x_b + 3y_b + z_b \\
  9x_c + 3y_c + z_c
\end{bmatrix}
\]

Using (4), the voltage vector of any inverter state can be achieved. Alternatively, the voltage vector diagram of the three-stage inverter is drawn by two superposition steps. First, the vector diagram of the three-level medium-voltage-stage inverter (composed of 19 vectors) is drawn at the end of each of the seven vectors of the high-voltage stage. Then, the vector diagram corresponding to the low-voltage stage has been superimposed at the ends of resultant vectors as shown in Fig. 2.

The modulation condition [17] has not been met by this design, that is, when controlling the inverter by PWM strategy, the medium- and high-voltage stages will be subjected to high switching frequency. However, the control strategy presented in this paper ensures that the high-voltage stage operate at fundamental frequency.

### 2.2 High- and medium-voltage-stage domains

Each of the 18-level inverter vectors can be represented by the addition of three vectors, one has a norm of 9Vs or 0Vs determined by \(x_{abc}\); the second has a norm of 6Vs, 3√3Vs, 3Vs or 0Vs determined by \(y_{abc}\) and the third has a norm of 2Vs, √3Vs, 1Vs or 0Vs determined by \(z_{abc}\). With the exception of the outmost vectors, most of the 18-level inverter vectors can be represented by more than one combination of the three-stage voltage vectors. For example, vector \(V_1\) shown in Fig. 2 is represented once as \(V_{h1} + V_{m1} + V_{l1}\) and second as \(V_{h1}^{'} + V_{m1}^{'} + V_{l1}^{'}\), where \(V_{hi}, V_{mi}\) and \(V_{li}\) are the voltage vectors corresponding to high-, medium- and low-voltage stages, respectively.

It is highly desirable for the switching frequency of the high-voltage stage to be reduced. The control algorithm explained in the next section aims to hold the high-voltage vector as long as the reference vector can reached through this high-voltage vector. We shall refer to the hexagonal area marked by the medium- and low-stage vectors superimposed on a given high-state vector by its ‘domain’. The seven domains of the high vectors are shown in Fig. 3. The figure shows that a high-state domain hexagon has a side length equivalent to 8Vs.

Dividing the space vectors area into domains is extended to the middle-stage vectors. Nineteen hexagons, each...
representing the area covered by low-voltage-stage vector diagram, can be drawn within each of the seven high-state domains at the tip of the 19 medium-voltage vectors. For illustration, one of the middle-state domain hexagons is shown in Fig. 3. With $x_{abc} = 100$ and $y_{abc} = 200$, the low-voltage-stage selection will cover the small hexagon marked at the rightmost side of Fig. 3; we shall refer to it as the domain of state [100, 200].

As shown in Fig. 3, within the grand hexagon some of the regions are covered by exactly one high-state domain without overlap (e.g. R1). If the reference vector is located in such area, the controller should select the corresponding high state. Other areas are overlaps of two or three high-state domains (e.g. R2 and R3); in this case, there is more than one option in the selection of $x_{abc}$. We have exploited this to minimise the switching actions at the higher voltage stages. The medium-state domains also overlap and this will be utilised in a similar way.

3 Control strategy

3.1 Control algorithm

During the $n$th sampling interval, the controller receives the input reference voltage vector and determines the switching signals based on the algorithm explained in this section. The switching signals determined during the $n$th sampling interval are applied to the switching devices during the $(n + 1)$th interval.

The switching state is determined as illustrated in the control algorithm flow diagram shown in Fig. 4. The calculation is carried out in three consecutive stages: high, medium and low stages. Each stage considers its previous
output in the calculation of its new state. The previous output is provided by the memory blocks ($Z^{-1}$).

### 3.2 High-voltage state determination

The calculation of $x_{abc}$ begins by finding out if the reference vector is located in the domain of the current high-voltage state. If so, $x_{abc}$ holds its value during the next switching interval. Otherwise, the ‘nearest’ high-voltage state is determined by first determining the reference voltage ‘sector’ and ‘zone’ defined in Figs. 5 and 6, respectively.

The zones have been defined based on the overlap of the domains of adjacent vectors. In Fig. 6, zones (1–4) are located in the domain of the zero state ($z$). Zones (2, 4, 5, 6) are in state $v$ domain and zones (3, 4, 6, 7) are in state $w$ domain. Table 1 defines the feasible next states for the general sector zones shown in Fig. 6. When the reference vector is located in a zone that is mutual between two or three domains, there is more than one next state option. In this case, the state reachable with minimum switching transition is the ‘nearest’ state to be selected. A lookup table of the nearest states has been used to determine $x_{abc}$.

<table>
<thead>
<tr>
<th>Reference vector zone</th>
<th>Feasible next state(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$z$</td>
</tr>
<tr>
<td>2</td>
<td>$v, z$</td>
</tr>
<tr>
<td>3</td>
<td>$w, z$</td>
</tr>
<tr>
<td>4</td>
<td>$v, w, z$</td>
</tr>
<tr>
<td>5</td>
<td>$v$</td>
</tr>
<tr>
<td>6</td>
<td>$v, w$</td>
</tr>
<tr>
<td>7</td>
<td>$w$</td>
</tr>
</tbody>
</table>

### 3.3 Medium-voltage state determination

The middle reference is calculated by subtracting the voltage vector corresponding to the next $x_{abc}$ from the input reference voltage vector. As in high-voltage state determination, the medium stage holds its state if the medium reference voltage is located within its domain; otherwise, the new medium switching state will be determined in a way similar to the determination of the high-stage state, but modified according to the three-level property.

The medium-stage zones for the general 60° sector are defined in Fig. 7. The 15 medium zones in a sector are determined by the overlap of the domains of the six vectors denoted in Fig. 7 by ($z$, $v'$, $v''$, $u$, $w'$ and $w''$).

When the medium reference is not within the domain of current state, the new state is calculated first by determining the medium reference vector sector and zone. This identifies the feasible next state or states, the states associated with the vectors having the reference located in their domains. When there is more than one feasible state,
the one reachable with minimum switching actions from the current value of \( y_{abc} \) is taken as the new \( y_{abc} \).

### 3.4 Low-voltage-state determination

The reference voltage for the low-voltage stage is determined by subtracting the vector corresponding to the calculated \( y_{abc} \) from the medium-stage reference vector, as shown in Fig. 4.

The low-stage zone corresponding to each of the low-voltage vectors has been defined as the nearest region to that vector as shown in Fig. 8. The control concept is to determine the zone at which the reference vector is located and operate the low-voltage stage in the corresponding state. If the vector is associated with two or three switching states, then the initial state will be considered to select the state reachable with minimum switching transitions.

The determination of the low-voltage zone has been carried out by three steps: axis transformation, dimensions rounding and polynomial interpolation. Following \( v-w \) axis system defined in Fig. 9, the reference vector \( (d_{ref}, q_{ref}) \) has been represented by its \( v-w \) components according to

\[
\begin{bmatrix} v_{ref} \\ w_{ref} \end{bmatrix} = \begin{bmatrix} 0.5 - \frac{\sqrt{3}}{2} \\ 0.5 + \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} d_{ref} \\ q_{ref} \end{bmatrix}
\]

In the determination of low-state zone, we are going to use the dimensions \( v_{ref} \) and \( w_{ref} \) besides \( d_{ref} \). The dimension rounding is performed to define the six nearest integer parameters

\[
\tilde{r}_{d,v,w} = \text{round}(d_{ref}, v_{ref}, w_{ref}) \quad (6)
\]

\[
\tilde{r}_{d,0,0} = \text{round}(d_{ref} + 0.5, v_{ref} + 0.5, w_{ref} + 0.5) \quad (7)
\]

Each of the 19 zones has a unique combination of three out of the six integer parameters defined in (6) and (7). For example, as shown in Fig. 9, if and only if the reference vector is located within zone 16, it will have \((-1.5 < d_{ref} < -0.5), (+0.5 < v_{ref} < +1.5) \) and \((-2.5 < w_{ref} < -1.5)\), and hence the integer rounding of \( d_{ref}, v_{ref} \) and \( w_{ref} \) are \(-1, +1 \) and \(-2, +2 \), respectively; we are going to use these three integers as identification parameters of zone 16.

When one of the zone diagonals is in the form \((d, v \text{ or } w = 1.5)\), then not all dimensions of all points in that zone will be rounded to the same integer. In this case, axis shifting by 0.5 is performed to have the dimensions of the shifted axis round to the same integer. This can be seen in zone 17 in Fig. 9, which has \((-0.5 < d_{ref} < +0.5), (+1.0 < v_{ref} < +2.0) \) and \((-2.0 < w_{ref} < -1.0)\). In this zone, the \( d \)-component of any vector located within has an integer rounding of 0. But the \( v \)-component is rounds to 1 or 2 while \( w \) is less or greater than 1.5, respectively. In this case, we are going to define the unique zone parameters using the shifted \( v \)-axis and, instead of \((+1.0 < v_{ref} < +2.0)\), we will consider \([+1.5 < (v_{ref} + 0.5) < +2.5]\), its rounding \( r_{v,2} = 2 \). Similarly \( r_{w,2} = -1 \). The unique combinations of the identification parameters of the 19 zones are given in Table 2.
For example, if the low reference vector $d-q$-axes are $1.3V_s$ and $-0.9V_s$, then its corresponding $v_{ref}$ and $w_{ref}$ will be, as calculated using (5), $v_{ref} \approx 1.43$ and $w_{ref} \approx -0.129$. The six rounded parameters for this reference are: $r_d = 1$, $r_v = 1$, $r_w = 0$, $r_d = 2$, $r_v = 2$ and $r_w = 0$. When compared to Table 2, we can see that the reference vector parameters matches only the identification parameters of zone $19$ $r_d$, $r_v$ and $r_w$.

After determining the six integer parameters corresponding to the reference vector, an interpolating polynomial is used to determine which zone these parameters match. The polynomial has the following form

$$\text{LowZone} = \sum_{i=1}^{19} I \ast P_i(\bar{r}_d, \bar{r}_v, \bar{r}_w, \bar{r}_d, \bar{r}_v, \bar{r}_w)$$

(8)

where $P_i$ is a product term that produces the value 1 when reference vector rounded dimensions $\bar{r}_d, \bar{r}_v, \bar{r}_w$ and $\bar{r}_d, \bar{r}_v, \bar{r}_w$ match the values of the $i$th zone; otherwise $P_i$ produces zero. $P_i$ has the following form (see (9))

$$P_i = \frac{\prod_{j=3}^{j=m-2} (\bar{r}_d(2) - j)^* \prod_{j=3}^{j=m-2} (\bar{r}_v(2) - j)^* \prod_{j=3}^{j=m-2} (\bar{r}_w(2) - j)\prod_{j=3}^{j=m-2} (\bar{r}_d(2) - j)\prod_{j=3}^{j=m-2} (\bar{r}_v(2) - j)\prod_{j=3}^{j=m-2} (\bar{r}_w(2) - j)}{\prod_{j=3}^{j=m-2} (\bar{r}_d(2) - j)\prod_{j=3}^{j=m-2} (\bar{r}_v(2) - j)\prod_{j=3}^{j=m-2} (\bar{r}_w(2) - j)}$$

(9)

In (9), at least one of the product terms at the numerator will be zero if the reference vector dimensions do not match all the three parameters of the $i$th zone. If the three parameters matched, the denominator will be equal to the numerator to bring the value of $P_i$ to one.

Following the zone determination, $z_{abc}$ will be the identified. This state is unique for zones $8–19$. For zones $1–7$, equivalent states associated with the zone are compared to the initial $z_{abc}$ and the state that can be reached with minimum switching actions is selected.

### 4 DSP implementation

The control algorithm has been implemented using DSP controller board cZdsp F2812. The 150 MHz, fixed-point, low-cost CPU executed the algorithm with a sampling frequency exceeding 25 kHz and using the on-chip memory only; this reflects the computational efficiency of the proposed algorithm.

One of the 16-bit input/output (I/O) interface ports has been allocated for the reference input. The 8 MSBs have been assigned as the reference voltage amplitude where the step dc voltage ($V_s$) is assumed to be equivalent to (10)h. With this scale, the maximum reference amplitude (FF)$_h$ is corresponding to reference amplitude that approximately equals to $15.94V_s$. This limit is justified by the fact that the maximum norm of reference vector located within the grant hexagon is $14.722V_s$. 

Figure 9 $v-w$-axis system with respect to the 19 low-stage zones
The reference amplitude of \((\text{EC})_h\) is considered to be the base amplitude or a reference of a magnitude control ratio, \(M = 100\%\).

The reference vector angle is represented by the 8-LSBs of the input and coded from (20) \(h\)-to-(DF) \(h\) as shown in Fig. 5.

The resolution of this representation is 1.875\%/bit compared to 2.83\%, the minimum angle between any two adjacent voltage vectors of the 18-level inverter; there is no loss of resolution by this representation. Further, this coding allows direct determination of the operating sector as the 3 MSBs and saves computation time.

A second 16-bit I/O interface port has been allocated for the switching signal output. Each arm of the two- and three-level sub-inverters is driven by 1 bit. External logic circuit has been used to decode the switching signals and insert blanking time.

### 5 Experimental results

A prototype of the proposed inverter has been constructed. The low- and medium-voltage stages have been supplied by a lead acid 12 V – 5.5 A \(h\) batteries. Three series-connected units are used for the medium-voltage stage to supply 36 V. The high-voltage stage has been fed by 108 V dc using a regulated power supply. For high- and medium-voltage stages, 600 V IGBTs are used, whereas MOSFETs have been used for the low-voltage stage. The experimental setup diagram is shown in Fig. 10. A three-phase induction motor of the following ratings has been used as a load:

- **Rated power:** 0.9 kW
- **Rated voltage:** 380 V
- **Rated speed:** 1420 rpm
- **Base frequency:** 50 Hz
- **Pole pairs:** 2

With magnitude control ratio of 80\%, 40 Hz reference frequency, 20 kHz controller's sampling frequency and the induction motor adjustable load are set to bring the motor

<table>
<thead>
<tr>
<th>Zone</th>
<th>(r_0)</th>
<th>(r_{d2})</th>
<th>(r_v)</th>
<th>(r_{v2})</th>
<th>(r_w)</th>
<th>(r_{w2})</th>
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</table>

The integer identifiers of the 19 low-state zones are shown in Fig. 11.

![Experimental setup configuration](image-url)
power factor close to 0.8; various measurements have been taken and shown in Fig. 11. The load-phase voltage and current are shown in Fig. 11a. The current is very close to pure sine wave, whereas the voltage quality is reflected in its spectrum shown in Fig. 11b where the highest harmonic forms about 1.07% of the fundamental. The dc supply and batteries’ currents are also given.

The main dc source current shown in Fig. 11c verifies that the high-voltage stage is operating in the square wave mode and that most of the real load power is supplied by the main dc source. Figs. 11d and 11e show the medium- and low-stage battery currents, indicating highly reactive current conditions. Bidirectional current capability is essential for the medium- and low-voltage stages, and in our implementation this has been realised by the batteries. However, full bridge converter units to rectify the outputs of isolated secondary windings have been considered as reversible DC supply by some multistage inverter designs [5, 6, 17]. This arrangement implies costly dc sourcing and high losses. Therefore the alternatives have been sought as in [4], where the low-voltage stage is fed using capacitors and the control strategy maintains the average power of this stage at zero. With the lower voltage stages fed with batteries, the regenerative capability of this inverter is inherent with $M \leq 0.47$, where the high-voltage stage operates in current freewheeling mode. This feature is suitable for two quadrant drives, which are usually designed with regenerative power that is only a fraction of the rated power.

Fig. 12 shows the fractions of the three stages in the formation of the total phase voltage with $M = 0.8$. This figure verifies that the high-voltage stage operate in the square wave mode, or with fundamental output frequency.
It can also be seen that the medium stage in this case operates at five times the fundamental frequency.

Fig. 13 shows the phase voltage waveforms and the total harmonic distortion (THD) for different values of the reference amplitude. The inverter voltage quality is affected at very low reference amplitude; however, with a reference input of 40% or higher the output voltage has THD less than 5%.

Table 3 compares the suggested system with four other designs and control methods. The comparison involves the number of switching devices, inverter levels, high-voltage-stage switching frequency and THD. It can be seen that the suggested design has the highest (level/switch) ratio and the lowest THD for $0.8 < M < 0.9$ compared to all the designs except for the 27-level three-stage asymmetrical inverter with selected harmonic elimination control. Recalling that the asymmetrical inverter requires three isolated main dc supplies for the high-voltage stage, the presented topology has considerably lower implementation cost. Furthermore, the technique of selected harmonic elimination requires offline calculations of the switching angles and provides scalar voltage control, whereas the presented control strategy does not require any lookup table and inherently a voltage vector control method.

6 Conclusion

In this paper, a three-stage, 18-level inverter and its innovated control strategy have been presented. The described strategy
exploits the inverter's high resolution to approximate any reference vector by one of inverter vectors. This method has proven to provide little distorted waveforms for wide range of reference magnitude. The suggested strategy has proven to be satisfactory for most applications. The experimental results reveal the quality merits of the proposed inverter. Batteries have been used for sourcing hints that the arrangement is suitable for vehicle drive applications.

7 References


