Individual-phase decoupled $P–Q$ control of three-phase voltage source converter

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Abstract: Individual-phase control has six control degrees of freedom: $P$- and $Q$-control for each phase. The six control degrees are applied to a distribution static compensator (D-STATCOM): (i) to support the AC voltages against voltage droop arising from weak transmission lines; (ii) to balance the active and reactive powers at the sending-end although the three-phase load is unbalanced; and (iii) to balance the voltages across the unbalanced load. A second contribution is a method to suppress DC voltage imbalance of D-STATCOM capacitors caused by zero sequence transients. Proof of concept is by simulations. The simulation tool used is EMTDC-PSAD.

Nomenclature

List of abbreviations

- AC: alternating current
- SPM: single phase active power measurement
- DC: direct current
- IGBT: insulated gate bipolar transistor
- PLL: three-phase phase-locked loop
- PCC: point of common connection
- S-PLL: single-phase PLL
- exp: exponential function
- FACTS: flexible AC transmission system
- Im: imaginary part of complex number
- D-STATCOM: distribution static compensator
- LPF: low pass filter
- VSC: voltage source converter
- rms: root mean square
- SPWM: sinusoidal pulse-width modulation
- PI: proportional-integral controller
- HVdc: high voltage direct current

Symbols with subscripts or superscripts

$M(t)$: modulation signal of SPWM
$f$: frequency
$m(t)$: compensated modulation signal of SPWM
$\theta$: phase angle
$\Delta V$: perturbation voltage
$\varepsilon$: error signal
$C(t)$: reference current of the VSC

Subscripts and superscripts

$+$/$-$/$0$: positive/negative/zero sequences
$a/b/c$: $a$-phase/$b$-phase/$c$-phase in abc frame
$d/q$: $d$ axis/$q$ axis in dq frame
$V_{a}$, $V_{b}$, $V_{c}$: voltages of $a$-, $b$- and $c$-phase
$*$: controlling variable
$T_{a}$, $T_{b}$, $T_{c}$: $a$-, $b$- and $c$-phase of transmission lines
$N$: neutral wire
$La$, $Lb$, $Lc$: $a$-, $b$- and $c$-phase of load
$\overline{ave}$: average value
$Sa$, $Sh$, $Sc$: $a$-, $b$- and $c$-phase of sending-end side
$Loss$: VSC losses
$Ca$, $Cb$, $Cc$: $a$-, $b$- and $c$-phase of D-STATCOM
$dc$: VSC DC link
$U$: upper bus of DC link
$Tri$: triangle carrier
$L$: lower bus of DC link
$REF$: reference values

Other symbols

$\omega$: radian frequency
$j$: imaginary axis in apparent plan
$K_p$: proportional gain
$K_i$: integral gain

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1 Introduction

1.1 Decoupled P–Q control

Voltage-source converters (VSCs) are the basic power electronic building blocks of motor drives [1, 2], direct current transmission systems (VSC–HVdc) and flexible AC transmission systems (FACTS) [3, 4]. Currently, decoupled P–Q control brings VSCs to a very high level of controllability [5]. This paper is concerned with presenting individual-phase control, a new method based on decoupled P–Q control of individual phases. Individual-phase control will be useful to electric railways and trams supplied by single-line pantographs [6]. It will be equally valuable when three-phase power systems have faults. Apart from faults, most domestic supplies are from a single phase and a neutral wire. In spite of continual effort to balance the three single-phase loads, the distribution bus is unbalanced most of the time. Since the distribution substation also supplies AC motors, voltage imbalance should not exceed 3%, although it is not an American National Standard Institute (ANSI) standard [7]. Balancing distribution loads allows the transmission lines to be loaded equally, thus increasing their power carrying capability. The balancing capability would allow VSCs to compete with the cheaper thyristor-based static var compensator (SVC), which is only capable of supporting against voltage droops.

Charles L. Fortescue’s symmetrical components, combined with instantaneous active and reactive power analysis [8–14], are applied widely to deal with asymmetrical operation. Although the symmetrical component method can deal with a large class of unbalanced problems, the underlying assumption is that the system is balanced, except for the fault, so that the system can be decomposed into positive, negative and zero sequence impedances. To broaden the methodology for solving imbalances, a preliminary form of the individual-phase control method has appeared in [15].

Conventional decoupled P–Q control presumes symmetrical operation, where a three-phase phase-locked loop (PLL) extracts the requisite information [sin ωt, cos ωt] from the balanced three-phase line voltages, to transform the voltages and currents in the a–b–c frame to the d–q frame [5]. In the d–q frame, the active and reactive powers are \( P = v_d(i_d^*) + v_q(i_q^*) \), \( Q = v_d(i_q^-) - v_q(i_d^-) \). When the PLL is locked on to the a-phase, \( v_d(t) = 0 \) so that \( P = v_d(i_d^*) \), \( Q = v_d(i_q^-) \). Thus, using the VSC to inject the current references \( i_d^* \) and \( i_q^* \), decoupled P–Q control is accomplished because \( P^* = v_d(i_d^*) \), \( Q^* = v_d(i_q^-) \). The symbol (*) is used to denote a control variable in this paper.

In this paper, individual-phase control makes use of three single-phase decoupled P–Q controllers: \( (P_{a}, Q_{a}) \), \( (P_{b}, Q_{b}) \) and \( (P_{c}, Q_{c}) \). To demonstrate the method, it is applied to a distribution static compensator (D-STATCOM) to balance asymmetrical loads as in [16, 17]. In the validation test, the unbalanced loads are connected to balanced three-phase transmission lines through IEEE 4 Node Test Feeder [18].

1.2 Contributions

The contributions of this paper are in:
- Presenting a new control method based individual phase decoupled P–Q control.
- Presenting a method which suppresses undesirable mid-point capacitor DC voltage imbalance caused by zero sequence DC current offsets in transients.

1.3 Organisation of text

The paper is organised as follows: Section 2 presents the method of individual-phase control. Section 3 applies the method to a D-STATCOM. Section 4 examines how the D-STATCOM can accommodate zero and negative sequence components. Section 5 presents the control of D-STATCOM using the block diagrams. Section 6 presents simulation results which validate the individual-phase control method. Discussion is presented in Section 7. Section 8 presents the conclusions.

2 Individual-phase control

2.1 Single-phase PLL (S-PLL)

Recently, through advances in signal processing theory [19–21], S-PLL has been claimed to be robust and reliable. The authors have used Fig. 1a as S-PLL with the notch filter of Fig. 1b to remove the 2nd harmonic. It is adapted from Fig. 2 of [21], the adaptation being the removal of the proportional-integral controller (PI) filter. The adaptation has been made after simulation tests show that the S-PLL of Fig. 1a is accurate and has fast enough time response. However, it should be pointed out that the tests in this paper are insufficient to prove robustness and reliability. From an input signal \( \sin(\omega t + \theta) \), the S-PLL acquires the
The conversion is based on producing the reference voltage and reference current to reference voltage conversion stage.

### 2.2 Defining phasors based on S-PLL

Using the $a$-phase, for example, its voltage

$$v_a(t) = \text{Im} \left[ \sqrt{2} V_a e^{j(\omega t + \theta)} \right] = \sqrt{2} V_a \sin(\omega t + \theta - \pi/2)$$

(1)

where ‘Im’ designates ‘imaginary’.

The S-PLL has acquired the angle $(\omega t + \theta - \pi/2)$ so that $\sin(\omega t + \theta - \pi/2)$ is the base of ‘in-phase’ component and $\cos(\omega t + \theta - \pi/2)$ is the base of ‘in-quadrature’ component. The $a$-phase phasor is therefore

$$\bar{V}_a = V_a$$

(2)

The $a$-phase current phasor

$$\bar{I}_a = I_{pa} + jI_{qa}$$

(3)

as a time function is

$$i_a(t) = \text{Im} \left[ \sqrt{2} I_a e^{j(\omega t + \theta - \pi/2)} \right] = \sqrt{2} [I_{pa} \sin(\omega t + \theta - \pi/2) + I_{qa} \cos(\omega t + \theta - \pi/2)]$$

(4)

### 2.3 Individual phase $P$–$Q$ quantities

The apparent power of the $a$-phase is

$$\Sigma_a = P_a + jQ_a = \bar{V}_a (I_{pa} - jI_{qa})$$

(5)

Substituting (2) in (5), the apparent power is

$$\Sigma_a = P_a + jQ_a = V_a I_{pa} - jV_a I_{qa}$$

(6)

Therefore by injecting a controlled current of the $a$-phase as

$$\bar{I}_a = \left( I_{pa}^* - jI_{qa}^* \right)$$

(7)

the controlled apparent power is

$$P_a^* + jQ_a^* = V_a (I_{pa}^* - jI_{qa}^*)$$

(8)

Decoupled $P$–$Q$ control of the $a$-phase consists of forming the reference current of the VSC as

$$C_a(t) = \sqrt{2} \left[ I_{pa}^* \sin(\omega t + \theta - \pi/2) - I_{qa}^* \cos(\omega t + \theta - \pi/2) \right]$$

(9)

VSC outputs voltage pulses from the modulating signals of sinusoidal pulse-width modulation (SPWM). To make the VSC track the reference current signal $C_a(t)$ of (9), there is a reference current to reference voltage conversion stage. The conversion is based on producing the reference voltage signal $M_a^*(t)$ by negative feedback of the error between the measured output current $i_a(t)$ and $C_a(t)$. Future work will apply advanced methods, such as ‘dead-beat control’.

### 2.4 Single-phase active power measurement (SPM)

Single-phase active power is obtained by multiplying instantaneous voltage and current measurements to form $v(t) \times i(t)$ and removing the double frequency term by a notch filter as shown in Fig. 2.

### 3 Managing apparent powers by individual-phase control

#### 3.1 Managing active power

For asymmetrical operation, this paper considers unequal load impedances $Z_{L_a}$, $Z_{L_b}$, $Z_{L_c}$ as shown in Fig. 3. The loads are connected to balanced sending-end voltage sources by balanced transmission-lines (impedances $Z_t$) through an IEEE 4 Node Test Feeder [18] (between Node #1 and Node #4). Details of the test feeder are listed in Section 11.2 in the appendix. The point-of-common coupling (PCC) of D-STATCOM is at Node 3. The 4th wire of the VSC joins its ground point to the ground points of the sub-station and the transformers.

The D-STATCOM redistributes the active powers, $P_{L_a}$, $P_{L_b}$, $P_{L_c}$ of the unequal load-side impedances so that the active powers to be supplied from the sending-end side are

$$P_{Sa} = P_{Sb} = P_{Sc} = P_\text{ave} + P_{\text{Loss}}/3$$

where $P_\text{ave}$ is the average active power of the three loads, that is

$$P_\text{ave} = P_{La} + P_{Lb} + P_{Lc}$$

(10)

and $P_{\text{Loss}}/3$ is the per phase power loss of D-STATCOM.

The D-STATCOM injects apparent powers

$$\Sigma_{Ca}^* = P_{Ca}^* + jQ_{Ca}^*$$

$$\Sigma_{Cb}^* = P_{Cb}^* + jQ_{Cb}^*$$

$$\Sigma_{Cc}^* = P_{Cc}^* + jQ_{Cc}^*$$

(12)

The active power components of D-STATCOM must satisfy

$$P_{Ca}^* = P_{Sa} - P_{L_a}$$

$$P_{Cb}^* = P_{Sb} - P_{L_b}$$

$$P_{Cc}^* = P_{Sc} - P_{L_c}$$

(13)

Negative feedback error, $\varepsilon_{P_a} = P_\text{ave} + P_{\text{Loss}} - P_{sa}$, is applied to control $P_{Ca}^*$ of (12). The same negative feedback control is applied to the other two phases. Ultimately, $\varepsilon_{P_b} = \varepsilon_{P_b} = \varepsilon_{P_c} = 0.0$ and the source-side active powers are equalised.

#### 3.2 Managing reactive power

In supporting AC voltage against sag, the AC ‘voltage magnitudes’ of the three phases are measured and compared
with the AC voltage references. The AC voltage errors of the phases are applied to the reactive power control of D-STATCOM \( \Phi_C \), \( \Phi_C^* \), \( \Phi_C^b \), \( \Phi_C^c \) of (12). When the errors are ‘nulled’ by the negative feedback, the voltage magnitudes of the three phases at the PCC are equalised.

Owing to three-phase balance in: (i) the sending-end voltages, (ii) the transmission line impedances \( Z_T \), (iii) the active powers \( P_{Sa}, P_{Sb}, P_{Sc} \) and (iv) the magnitudes of the AC voltages, the angles of three-phase voltages at the PCC are balanced. This is accomplished without the necessity of taking single-phase reactive power measurements.

4 Implementation by VSC

The D-STATCOM is implemented by a four-wire, three-phase VSC shown in Fig. 4. The 4th wire from M is connected to the same ground points of the neutral of the wye connected transformers and the sub-station in Fig. 3. As the properties of the VSC are well known, the points which require further attention are in the handling of: (i) zero sequence and (ii) the negative sequence which arise from asymmetrical operation.

4.1 Zero-sequence current

Zero-sequence current is accommodated by grounding M, the midpoint of the capacitors as shown in Fig. 4. The voltages across the mid-point capacitors become unbalanced by zero sequence currents and this can lead to distorted AC voltage outputs [22, 23].

It is well known that the zero-sequence current on entering the VSC of Fig. 4 from the AC-side, splits into two equal halves: \( i_N(t) = i_U(t) - i_L(t) \) and exits as \( i_N(t) \). Thus, the zero-sequence charges \( v_U(t) \) and discharges \( v_L(t) \) by the same amount but in opposite polarity.

By applying Kirchhoff’s current law at point M in Fig. 4

\[
i_N(t) = i_U(t) - i_L(t)
\]  

The neutral current, \( i_N(t) \), flows through the ground. The imbalance in capacitor voltages can be expressed by

\[
\Delta V = v_U(t) - v_L(t) = \frac{1}{C} \int i_U(t) \, dt - \frac{1}{C} \int i_L(t) \, dt
\]

Substituting (14) in (15), the imbalance voltage is

\[
\Delta V = \frac{1}{C} \int (i_U(t) - i_L(t)) \, dt = \frac{1}{C} \int i_N(t) \, dt
\]

As AC zero-sequence current because of load imbalance has to be admitted into the VSC, \( \Delta V \) can only be reduced by increasing the size of the mid-point capacitors.

4.2 Mid-point capacitor DC voltage imbalance

What is undesirable is the integral of the zero-sequence DC offset (homogeneous parts of differential equations) of transients. On integration (16), they cause DC voltage imbalance as illustrated in Fig. 5a. Since the point M in Fig. 4 is the ground voltage of the AC phases, the AC voltages will not be symmetrical with respect to ground.

4.3 Suppressing DC voltage imbalance of mid-point capacitors

The imbalance can be suppressed by producing zero-sequence currents in the direction opposite to the zero-sequence currents which produced it in the first place.

Fig. 3  Asymmetrical loads \( Z_{La}, Z_{Lb}, Z_{Lc} \) connected to symmetrical transmission lines \( Z_T \) by IEEE 4 Node Test Feeder. D-STATCOM connected to node #3

Fig. 4  Three-phases VSC
This is done through the ‘balancing mid-point capacitors’ block in Fig. 6 which will be explained in Section 5.7. For the present, the experimental result in Fig. 5b shows that the capacitor voltages can be equalised by the balancing mid-point capacitors block of Fig. 6.

4.4 Double line frequency voltage component because of negative sequence

As is well known the presence of negative sequence gives rise to a double frequency term in voltage across the DC buses $v_{dc}(t)$.

4.5 Compensating double frequency voltage ripple in SPWM

In SPWM, the fundamental component of the pulsed voltage at the terminal of the $a$-phase of the VSC is

$$v_a(t) = \frac{m_a^*(t)v_{dc}(t)}{2V_{tr}} \quad (17)$$

where $m_a^*(t)$ is the modulating signal and $V_{tr}$ is the peak of the triangle carrier of SPWM. When $v_{dc}(t)$ is no longer a constant, the VSC ceases to be a linear amplifier of its modulating signal.

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Fig. 5  Experimentally measured voltages across upper and lower mid-point capacitors because of DC component in zero-sequence current

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Fig. 6  Decoupled P–Q control of $a$-phase
signal and \(v_a(t)\) becomes distorted. The solution adopted is taken from [24]. When the ‘intended’ modulating signal is \(M'_a(t)\), D-STATCOM is immunised against DC voltage fluctuation by measuring \(v_{a}(t)\) and modifying the modulating signal as

\[
m_a^*(t) = \frac{M'_a(t)V_{dc-REF}}{v_a(t)}
\]

(18)

With this compensation

\[
v_a(t) = \frac{M'_a(t)V_{dc-REF}}{2V_r}
\]

(19)

retains the linearity of SPWM.

5 Control to balance asymmetrical loads

Fig. 6 is the control block diagram of the \(a\)-phase. Control blocks, which are common to the \(b\)- and \(c\)-phase also, are surrounded by ‘hatched lines’. The gains of all PI blocks have been fine-tuned by control theory analysis together with trial and error adjustments.

5.1 Formation of \(P_{ave}\) of (10)

\(SPM_{la}, SPM_{lb}\) and \(SPM_{lc}\) (of Fig. 2) measure the load-side active powers \(P_{la}, P_{lb}\) and \(P_{lc}\) which are summed to form the average power, \(P_{ave}\).

5.2 Replenishing Ohmic losses in VSC

In the shaded box, the DC voltage regulator feedback loop estimates \(P_{Last}/3\) from the error \(\varepsilon_{dc} = V_{dc-REF} - V_{dc}\). \(V_{dc}\) is obtained by passing \(V_{dc}(t)\) through a low pass filter (LPF) to remove the 2nd harmonic.

5.3 Active power control of individual phase

\(P_{sa}\) is measured, compared with \(P_{ave} + P_{Last}\) and the error is applied to the active power controller \(I_{qa}\) of (7) and (8).

5.4 Reactive power control of individual phase

The root mean square (rms) value of AC voltage, \(V_o\), is measured, compared with the reference \(V_{a-REF}\) and the AC voltage error, \(\varepsilon_{V} = V_{a-REF} - V_o\), after passing the PI block is applied to \(I_{qa}\) of (7) and (8).

5.5 Individual phase control

From the S-PLL of Fig. 1, \((\omega t + \theta_{V-a})\) of the \(a\)-phase is measured. After forming \(\sin(\omega t + \theta_{V-a})\) and \(\cos(\omega t + \theta_{V-a})\), they are multiplied to \(I_{qa}\) and \(I_{qb}\) to form the reference current signal \(I_{a}(t)\) of (9).

5.6 Balancing DC capacitors voltages

In the shaded box of Fig. 6, the lower DC bus voltage \(v_1(t)\) passes through LPF to ensure that ‘only’ DC voltage imbalance because of the DC component of zero-sequence transients (see Fig. 5) is suppressed. The output is compared with 0.5 \(V_{dc}\). The error \(\varepsilon_{dc} = 0.5V_{dc} - V_{L}\) (after passing through a proportional gain, \(K_p\)) goes to \(a\)-, \(b\)- and \(c\)-phase to produce together a zero-sequence current which reduces the error \([0.5V_{dc} - V_{L}]\) to zero. For the \(a\)-phase, the error, \(\varepsilon_{dc} = 0.5V_{dc} - V_{L}\), is added to the signal \(C_a(t)\) to form the reference current signal. The reference current signal \(C_a(t)\) is converted to reference voltage signal \(M'_a(t)\).

5.7 Compensating for fluctuation of \(v_{dc}(t)\)

To compensate for DC voltage fluctuation because of double frequency voltage ripple, \(M'_a(t)\) is modified as in (18) by multiplying \(V_{dc-REF}\) and \(1/V_{dc}(t)\) to form \(m_a^*(t)\) of SPWM.

6 Validation by simulations

6.1 Model of test system

In the IEEE 4 Node Test Feeder of Fig. 3 [18], the delta/wye transformer is connected between Node 2 and Node 3. The impedances of the pole lines between Node 1 and 2 and between Node 3 and 4 are asymmetrical. As individual-phase control cannot handle the two asymmetries from two sides of the transformer, the adaptation taken in the test is to assume the impedances between Node \#1 and Node \#2 to be ‘symmetrical’. This means that pole lines are not used on the high-voltage side. On the low-voltage side of the transformers, induction motors and synchronous generators are supplied at higher voltages than residential loads. They are usually connected by balanced three-phase lines from the PCC, where the D-STATCOM can balance the AC voltages. The asymmetrical impedances between Nodes 3 and 4 are labelled as \(Z_{La}, Z_{Lb}, Z_{Lc}\) and are lumped together with the load impedances \(Z_{La}, Z_{Lb}, Z_{Lc}\). PSCAD has a software, which handles the asymmetric impedances of IEEE 4 Node Test Feeder, and it has been used.

The bases of per unitisation and the parameters used in the power system of Fig. 3 and the D-STATCOM are listed in Table 1 in Section 11.1, of the appendix.

6.2 Test objectives – unbalanced loads and faults

In addition to the three objectives described in the Introduction, the simulation tests have also been planned to demonstrate the capability to balance a succession of imbalances from different kinds of faults using the same control strategy. The faults are: (a) loss of a load line (opening of circuit breaker C); and (b) line-to-line short circuit (closing of circuit breaker D through impedance \(Z_3\)).

6.3 Simulation results

Fig. 7 presents the simulation results of: (a) the magnitudes of the line-to-ground voltages at the PCC; (b), (c) the active and reactive powers, respectively, at the sending-end; (d), (e) the active and reactive powers, respectively, on the load side of the PCC; (f), (g) the active and reactive powers, respectively, of D-STATCOM. Fig. 8 presents the apparent power of D-STATCOM. Fig. 9 shows the negative and zero-sequence of the voltage at the PCC. For the per-unitisation used, 1.0 pu voltage = (voltage base)/\(\sqrt{3}\); 1.0 pu active or reactive power = (MVA base)/3.

Sub-period: \(1.0 \leq t < 2.0 \text{s}\): The AC voltage support of D-STATCOM is not activated. The voltage droops shown in Fig. 7a show that three unequal voltage magnitudes are in need of voltage support.

Sub-period: \(2.0 \leq t < 3.0 \text{s}\): The ‘AC voltage support’ of D-STATCOM is activated. Fig. 7a shows that voltage
magnitudes are supported and equalised for $t \geq 2.0$ s. Owing to the increase in voltage magnitudes at the PCC, the three unequal active and reactive powers increase as shown in (b), (c) and (d), (e).
Sub-period: $3.0 \leq t < 4.0$ s: At $t = 3.0$ s, the ‘balancing control’ is activated. The active and reactive powers in (b) and (c) on the sending-end become equal. Comparing the same graphs with those for the previous sub-period, $2.0 \leq t < 3.0$ s, both the active and reactive powers of the three-phase transmission lines are lower. The reduced apparent power is desirable because the transmission lines can transmit more active power.

Sub-period: $4.0 \leq t < 5.0$ s: In opening circuit breaker C to simulate loss of one load line, $P_{lb}$ and $Q_{lb}$ of the b-phase fall to zero as shown in (d) and (e).

Sub-period: $5.0 \leq t < 6.0$ s: At $t = 5.0$ s, circuit breaker C is closed and circuit breaker D is closed to connect impedance $Z_D$ across a-phase and c-phase to simulate a line-to-line fault. For $3.0 \leq t < 6.0$ s, the capability of the control of D-STATCOM to balance the active and reactive power on the sending-end is demonstrated in (b) and (c).

Fig. 8 shows the MVA required of each phase of D-STATCOM. In this example, supporting the voltage against droop ($2.0 < t < 3.0$ s) represents the dominant cost. Balancing severe asymmetry because of loss of a line is not demanding because the load requirement is reduced by one-third. Equalising the load power ($3.0 < t < 6.0$ s) even for severe fault does not require a high differential price to pay over the cost of voltage droop support.

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$V_\theta$ $V_\nu$

Fig. 9 Negative and zero-sequence voltage components at the PCC, pu

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$V_\theta$ $V_\nu$

Fig. 8 Apparent powers for each phase of D-STATCOM, pu

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$V_\theta$ $V_\nu$

Fig. 10 Sending-end side

a Three-phase currents, pu

b Computed negative and zero-sequence currents, pu
Fig. 9 shows that except for the switching transients, the computed negative and zero sequence voltage components are zero at the PCC, for $3.0 \, \text{s} < t < 6.0 \, \text{s}$. Fig. 9 is needed to prove that the voltage angles at the PCC are balanced sending-end side of the PCC before and after switching at $t = 4.0 \, \text{s}$. The computed instantaneous negative and zero sequence currents in (b) show that the D-STATCOM has successfully balanced the asymmetry in the load except for the duration of the switching transient. The mid-point capacitor DC voltage imbalance in Fig. 5a has origins from switching transients of the zero sequence shown in Fig 10b. The duration of the transient depends on the time constants of circuit elements in the VSC, the network and the transformer.

7 Discussion

Although D-STATCOM is a reactive power controller, it is possible to use it to redistribute active power from one phase to another phase. This is because the active powers in (13) sum to zero as a consequence of (10) and (11). This is clearly shown in Fig. 7 which shows that the active powers of the three phases of D-STATCOM sum to zero at every time instant.

8 Conclusions

This paper has presented a new control method based on individual phase decoupled $P-Q$ control. Simulation tests show that a D-STATCOM operating under individual phase control can fulfill multiple balancing objectives simultaneously using a single control strategy for a series of imbalances

(i) the load is unbalanced;
(ii) the load is unbalanced and has lost one load line;
(iii) the load is unbalanced and has a line-to-line fault across two load lines.

This paper has presented a method of balancing mid-point capacitors which enables the D-STATCOM to cope with zero sequence DC offsets arising from transients.

9 Acknowledgment

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10 References

GMR = 0.0244 ft., resistance = 0.306 Ω/mile, diameter = 0.721 in.
Neutral conductor: 4/0 6/1 ACSR
GMR = 0.00814 ft., resistance = 0.592 Ω/mile, diameter = 0.563 in.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Base quantities and system parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>base quantities</td>
<td>$S_{base}$</td>
</tr>
<tr>
<td></td>
<td>$V_{baseHV}$</td>
</tr>
<tr>
<td></td>
<td>$Z_{baseHV}$</td>
</tr>
<tr>
<td></td>
<td>$V_{baseLV}$</td>
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<tr>
<td></td>
<td>$Z_{baseLV}$</td>
</tr>
<tr>
<td>load and line parameters</td>
<td>$Z_{L_a}$, pu</td>
</tr>
<tr>
<td></td>
<td>$Z_{L_b}$, pu</td>
</tr>
<tr>
<td></td>
<td>$Z_{L_c}$, pu</td>
</tr>
<tr>
<td></td>
<td>$Z_{O}$, pu</td>
</tr>
<tr>
<td></td>
<td>$Z_{T}$, pu</td>
</tr>
<tr>
<td>transformer parameters</td>
<td>$S$ (connection)</td>
</tr>
<tr>
<td></td>
<td>$V_{HV}$</td>
</tr>
<tr>
<td></td>
<td>$V_{LV}$</td>
</tr>
<tr>
<td></td>
<td>$X_{Leakage}$, pu</td>
</tr>
<tr>
<td></td>
<td>$R_{loss}$, pu</td>
</tr>
<tr>
<td></td>
<td>$V_{b}$, pu</td>
</tr>
<tr>
<td>D-STATCOM parameters</td>
<td>$S_{D-STATCOM}$</td>
</tr>
<tr>
<td></td>
<td>$f_{Switching}$</td>
</tr>
<tr>
<td></td>
<td>$X_{Interface}$, pu</td>
</tr>
<tr>
<td></td>
<td>$V_{dc-REF}$, pu</td>
</tr>
</tbody>
</table>

Fig. 11 IEEE 4 Node Test Feeder

Fig. 12 Pole configuration