A Configurable Architecture for Fast Moments Computation

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Abstract
In this paper, we present a single-chip architecture for generating a full set of geometric moments using digital filters. Other types of moments such as Zernike and Tchebichef moments can also be implemented. The architecture can be configured for any order of geometric moments and image spatial resolution at run time. The use of a single-scaler method and reusable hardware resources enables higher order moments to be computed. The incorporation of two-level pipelining and masking techniques further increases the throughput. Realized in a field-programmable gate array, the design is capable of processing sixty $512 \times 512$ 8-bit-pixel images per second at 20 MHz, generating $(59 + 59)$ orders of geometric moments (3,600 moments). The maximum round-off error is approximately 1 %.

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**Keywords** Image processing · Moments · Digital filters · 
Real-time · Configurable · High-order · Field-Programmable
Gate Array (FPGA)

1 Introduction

Moment invariants first introduced by Hu [1] have been
extensively used in object classification, image, shape analy-
ses etc. [2–4]. Teague [3] later introduced a set of continuous
orthogonal moments, such as Zernike and Legendre moments.
Due to their orthogonality, they found a wider range of applica-
tions, which include character recognition, trademark seg-
mentation, and retrieval [5, 6]. Further work has led to the

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2 Review of the Digital Filters

GM, $m_{pq}$, of order $(p+q)$, of a digital image $f(x,y)$
spatial resolution of $N \times M$ is defined as:

$$m_{pq} = \sum_{x=0}^{N-1} \sum_{y=0}^{M-1} f(x,y) x^p y^q.$$  

To calculate (1), Hatamian [16] proposed a 2-
method to implement the first 16 moments. Wong
[17] moved the delay element in the basic filter struc-
to the feedback path, for up to the third order. Kotz
Andreidis [18, 19] extended the basic filter structure
incorporating a single-pole, feedback type of filter
as shown in Fig. 1a. The maximum (max) values of the

data arrives. Next, we introduce a design to ad-
aforementioned shortcomings.

3 Overview of the Design

The top-level diagram in Fig. 2 comprises the t-
modules of the design: the digital filter and the mat-
plication modules. The modules are connected by an
ite Random-Access Memory (RAM), which is
mediate data and scale-factors. In this design,
adders and other associated circuitry are collecti-
the cascaded filter structures. As is in [16], ima
to be first reversed.

An external host ensures that valid run-time con-
parameters have been written before asserting the
filtering signal. The moment generator issues the in-
signal to the host to signal its readiness for the next in-
host indicates the arrival of the next image by ass-
start new filtering signal. By using this mecha-

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Later, Kotoulas and Andreadis [20] improved on the filter structure in [16]. A single-pole, feedforward type of the filter structure shown in Fig. 1b is used. The propagation delay can now be ignored, as the outputs of the adders are registered. However, the size of the accumulator grid structure still increases significantly with the increasing maximum order of moments [18–20], and presents challenge to the routing. Other drawbacks include the insufficient time for the filters to output the results before the next row of input

Figure 2. Top-level architecture.

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