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A Configurable Architecture for Fast Moments Computation

Abstract

In this paper, we present a single-chip architecture for generating a full set of geometric moments using digital filters. Other types of moments such as Zernike and Tchebichef moments can also be implemented. The architecture can be configured for any order of geometric moments and image spatial resolution at run time. The use of a single-scaler method and reusable hardware resources enables higher order moments to be computed. The incorporation of two-level pipelining and masking techniques further increases the throughput. Realized in a field-programmable gate array, the design is capable of processing sixty 512 × 512 8-bit-pixel images per second at 20 MHz, generating (59 + 59) orders of geometric moments (3,600 moments). The maximum round-off error is approximately 1 %.

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A Configurable Architecture for Fast Moments Computation

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Abstract In this paper, we present a single-chip architecture for generating a full set of geometric moments using digital filters. Other types of moments such as Zernike and Tchebichef moments can also be implemented. The architecture can be configured for any order of geometric moments

introduction of a new set of discrete orthogonal n
Hahn, Tchebichef and Krawtchouk moments [7–9]. F
putational methods have also been developed [10–1
result, applications involving moments of as high as (
are becoming increasingly feasible [13–15]. Notwith

and image spatial resolution at run time. The use of a single-scaler method and reusable hardware resources enables higher order moments to be computed. The incorporation of two-level pipelining and masking techniques further increases the throughput. Realized in a field-programmable gate array, the design is capable of processing sixty 512×512 8-bit-pixel images per second at 20 MHz, generating (59+59) orders of geometric moments (3,600 moments). The maximum round-off error is approximately 1 %.

Keywords Image processing · Moments · Digital filters · Real-time · Configurable · High-order · Field-Programmable Gate Array (FPGA)

1 Introduction

Moment invariants first introduced by Hu [1] have been extensively used in object classification, image, shape analyses etc. [2–4]. Teague [3] later introduced a set of continuous orthogonal moments, such as Zernike and Legendre moments. Due to their orthogonality, they found a wider range of applications, which include character recognition, trademark segmentation, and retrieval [5, 6]. Further work has led to the

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the availability of fast algorithms, the computation t represents a challenge for real-time systems, for thei tions have largely been confined to the software don

Since Zernike [3], Tchebichef [8] and Krawtcl moments are shown to be realizable by computing metric Moments (GM), our motivation has been to run-time configurable, high-order GM computation ture using the extended digital filter structures. In section, we will review the digital filters structures. view of the design is provided in Section 3. In Secti single-scaler and cascaded filter structures will be d with the implementation results and performance presented in Section 5. We will conclude the pre in Section 6.

2 Review of the Digital Filters

GM, m_{pq}, of order $(p+q)$, of a digital image $f(x,y$ spatial resolution of $N \times M$ is defined as:

$$m_{pq} = \sum_{x=0}^{N-1} \sum_{y=0}^{M-1} f(x,y)\, x^p y^q.$$

To calculate (1), Hatamian [16] proposed a 2- method to implement the first 16 moments. Wong [17] moved the delay element in the basic filter struc to the feedback path, for up to the third order. Koto Andreadis [18, 19] extended the basic filter structure incorporating a single-pole, feedback type of filter as shown in Fig. 1a. The maximum (max) values of *the*

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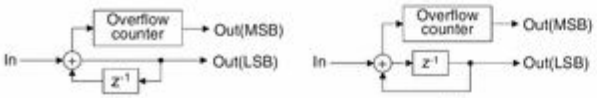


Figure 1 Kotoulas and Andriadis' basic filter structures. **a** Feedback type; **b** Feedforward type.

moment order and/or image spatial resolution (hereinafter referred to as run-time configurable parameters), are limited by the propagation delay along the serially connected adders in the filters. Due to the absence of a registered output for each of the adders, timing critical paths exist for relatively low maximum values of the run-time configurable parameters. When the same design is adapted for column filtering operations, even if all the outputs of the cascaded filter structures are available at the same time, an intermediate memory buffer may still be required for storing their outputs prior to the matrix multiplication operations. As memories have limited data ports, delays are inevitable anyway

data arrives. Next, we introduce a design to add aforementioned shortcomings.

3 Overview of the Design

The top-level diagram in Fig. 2 comprises the tv modules of the design: the digital filter and the matr plication modules. The modules are connected by an diate Random-Access Memory (RAM), which st intermediate data and scale-factors. In this design, adders and other associated circuitry are collectivel as the cascaded filter structures. As is in [16], ima to be first reversed.

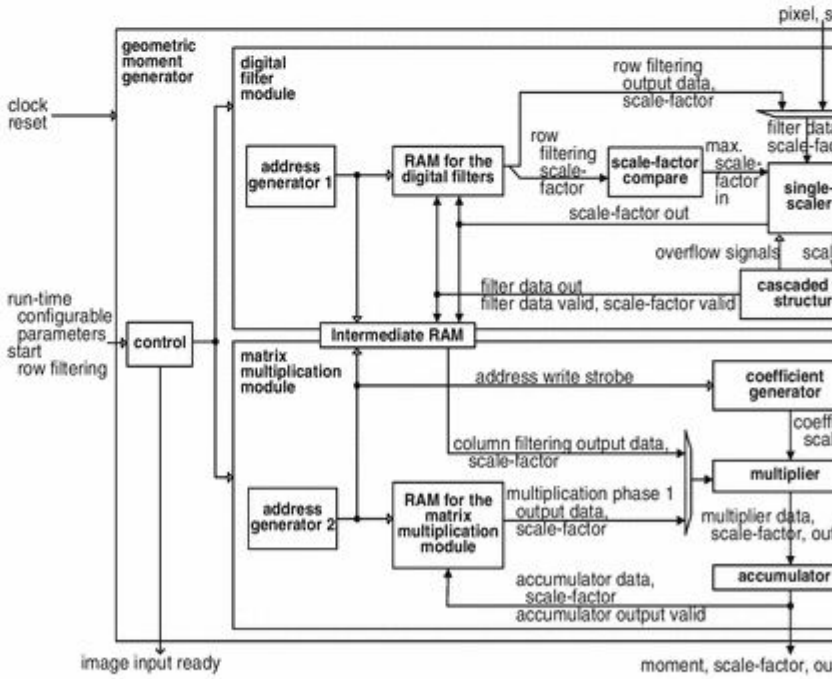
An external host ensures that valid run-time con parameters have been written before asserting the filtering signal. The moment generator issues the inp signal to the host to signal its readiness for the next im host indicates the arrival of the next image by asse start row filtering signal. By using this handshak

limited data ports, delays are inevitable anyway.

Later, Kotoulas and Andreadis [20] improved on the filter structure in [16]. A single-pole, feedforward type of the filter structure shown in Fig. 1b is used. The propagation delay can now be ignored, as the outputs of the adders are registered. However, the size of the accumulator grid structure still increases significantly with the increasing maximum order of moments [18–20], and presents challenge to the routing. Other drawbacks include the insufficient time for the filters to output the results before the next row of input

start row filtering signal. By using this handshak storing the intermediate data, we have discarded the adders and time-shared the row adders. At the en column filtering operation, the cascaded filter struct put the final filter output data to the intermediate RA accessed by the matrix multiplication module, which rates a multiplier, an accumulator, and a coefficient that generates the coefficients [21] used in the two matrix multiplication. After a given latency that de the run-time configurable parameters, the moment va

Figure 2 Top-level architecture.



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3. Overview of the Design

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