On the effects of NBTI degradation in p-MOSFET devices

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ABSTRACT

This paper presents the effects of interface trap concentration and threshold voltage shift on NBTI degradation in p-MOSFETs. To explore the degradation mechanisms, transistors having an EOT of 1.1 nm and 5 nm were simulated by applying various stress conditions. The NBTI degradation mechanism was studied by varying the gate voltage, temperature and substrate doping level. The simulations show NBTI degradation in terms of the threshold voltage shift, $\Delta V_{th}$ and number of interface traps, $N_{it}$. The simulation results show an improved degradation trend in terms of $\Delta V_{th}$ and $N_{it}$ when the substrate doping level is increased.

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1. Introduction

In recent years, Negative Bias Temperature Instability (NBTI) has become an important reliability issue which is a threat to device performance as it affects the lifetime of p-MOSFETs. In sub-micron technology, due to declining oxide thickness and channel width of p-MOSFETs, NBTI has become a major reliability concern [1]. In this research, we studied the nature of NBTI degradation by applying a constant gate voltage while we set the drain to source voltage to zero. From this study, we found an adverse effect on the reliability of p-MOSFETs at elevated temperatures and small oxide thickness [1–3]. This adverse effect may cause transistor failure as threshold voltage, drain current, subthreshold slope, transconductance and mobility will be shifted from their original values [2,3].

To solve the NBTI issue, researchers have reported different degradation models. One of the proposed degradation models is the reaction-diffusion model (R-D model) of Jeppson and Svensson [4]. This model explains the dependency of NBTI induced degradation on p-MOSFET transistors due to negative gate voltage and high temperature. This model explains the de-passivation of dangled and broken Si–H bonds. These dangled and broken bonds form an interface trap [5,6] $N_{it}$, which is important in determining the degradation mechanism. The generation rate of $N_{it}$ is expressed in Eq. (1):

$$\frac{dN_{it}}{dt} = k_f [N_0 - N_{it}] - k_r N_{it} N_{H}^0$$

where, $N_0$ is the initial number of Si–H bonds, $N_{it}$ is the interface trap concentration, and $N_{H}^0$ is the number of atomic hydrogen at Si–SiO2 interface, while $k_f$ and $k_r$ are Si–H bond breaking and recovery rates, respectively. In this paper, the NBTI degradation effect is simulated and studied using Modeling Interface-defect Generation (MIG) [7]. The simulation is based on different effective oxide thicknesses (EOT), different substrate doping levels and different stress conditions.

2. Simulation conditions

We performed the simulation process by considering the stress voltage as DC and the diffusion species as atomic hydrogen. Two p-MOSFETs with different EOT of 5 nm and 1.1 nm were employed, respectively. Four different concentrations of substrate doping were simulated, which varied from $5 \times 10^{16}$ cm$^{-3}$ to $1 \times 10^{18}$ cm$^{-3}$. Stress voltages and temperature were changed systematically to analyze transistor characteristics. The applied stress voltage was kept between $-2$ V and $-3.5$ V and the stress temperature was kept between 70 °C and 150 °C. The accuracy of the simulation was checked by keeping a harmony with the power law while a degradation slope of 0.25 was obtained due to the diffusion of atomic hydrogen [8,9].

3. Simulation results

3.1. Effect of substrate doping level in NBTI degradation

To examine the effects of threshold voltage shift ($\Delta V_{th}$) for different substrate doping levels, we simulated devices with smaller and larger EOT with a stress gate voltage of $-1$ V and a...
temperature of 100 °C, respectively. As per the simulation results in Fig. 1(a) and (b), when the substrate doping level increases, \( \Delta V_{th} \) decreases linearly following a power law [10]. However, the result obtained from Fig. 1(b) demonstrates a slight shift in slope for thicker EOT. This occurs as the amount of tunneling carriers becomes less for thicker oxide [11].

To investigate the effect of \( \Delta N_{it} \) for different substrate doping levels, devices having small and large EOT values were muted by applying a gate voltage of \(-1\) V at 100 °C. As shown in Fig. 2(a) and (b), \( \Delta N_{it} \) increases as the substrate doping level decreases. Due to decreasing doping level, \( \Delta V_{th} \) reduces and device lifetime increases [12]. This is due to the interrelation of \( \Delta V_{th} \) with subsequent changes in the interface states \( \Delta N_{it} \). The contribution of interface trap creation towards the threshold voltage shift was clearly explained by Schroder [13]. The same \( \Delta N_{it} \) slope, \( n \sim 0.25 \) was observed for both devices with small and large EOT, respectively. The similar \( \Delta N_{it} \) slopes are related to NBTI, which is caused due to hydrogen species as reported in Ref. [8,9].

3.2. Effect of stress temperature in NBTI degradation

To examine the effect of temperature dependence on NBTI degradation, transistors with EOT 1.1 nm and EOT 5 nm were simulated at fixed stress gate voltage with different stress temperature. The simulation results are shown in Fig. 3(a) and (b). The slopes are in the range of 0.2–0.25, in agreement with Refs. [8,9]. This behavior also indicates the diffusion species is atomic hydrogen. \( \Delta N_{it} \) shows a temperature dependence in that as the temperature increases, \( \Delta N_{it} \) increases. This can be explained by [3] based on the Arrhenius relation with diffusion rates affected by temperature variation, where the generation of \( \Delta N_{it} \) is dependent on the number of broken Si–SiO\(_2\) bonds. This mechanism was supported by Ref. [14] where the \( \Delta N_{it} \) creation is strongly dependent on temperature.

3.3. Effect of stress gate voltage in NBTI degradation

Fig. 5(a) and (b) show the graphs for \( \Delta N_{it} \) for EOT = 1.1 nm and EOT = 5 nm, at constant temperature with different gate voltages. There has been considerable debate regarding the voltage or field dependence of NBTI degradation and it was concluded that transistors with SiO\(_2\) normally experience a field dependent process [15]. From this we propose that the oxide field is an important factor in NBTI degradation. This work finds that devices with smaller EOT experience more degradation than devices with
larger EOT [16]. For both transistors, the interface trap concentration increases as the stress voltage increases. This shows an elevated NBTI effect at higher stress voltage. To ensure the stability of device performance at high bias voltage, CMOS devices with advanced processing are required along with the incorporation of spike-annealed laser devices [17].

4. Conclusion

NBTI is one of the major aspects of p-MOSFET reliability and considering this fact we have investigated the effects of NBTI caused by process and stress variation. Substrate doping concentration, EOT, stress voltage and temperature were varied and their effect on threshold voltage presented.

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