FPGA-based ASIC design of the three-phase synchronous PWM flyback converter

A.M. Omar and N.A. Rahim

Abstract: The design and development of a synchronous pulse-width modulation (PWM) generator suitable for the three-phase flyback converter is presented. The design is based on the Xilinx chip XC4005E field programmable gate array (FPGA). Two 30° of sine waveforms with two different carrier waveforms are used to generate the PWM. The PWM pattern proposed occupies less FPGA block cell, hence more space can be used for other control circuitry. The proposed technique enables the modulation index and the displacement factor to be changed externally. Results are provided to demonstrate the effectiveness of the design.

1 Introduction

Pulse width modulation (PWM) is a widely used technique for controlling the output of static power converters. By using PWM techniques, the frequency spectrum of the input waveforms can be changed such that major nonfundamental components are at relatively high frequency. PWM for the control of three-phase power converters can be performed using a variety of different methods. There are various control strategies for controlling the power factor and the fundamental current waveform. They have different implementations, dynamics responses, PWM patterns and harmonics content [1–3].

Generally, two classes of PWM techniques can be identified: (i) optimal PWM (ii) carrier PWM. The optimal PWM technique for producing switching patterns is based on the optimisation of specific performance criteria [3]. In this case, the converter switching patterns are calculated *a priori* for given operating conditions and are then stored in memory (look-up tables) for use in real time. Reduction in converter effective switching frequency is achieved, and higher gain due to over-modulation is possible when compared with the conventional PWM scheme. However, the considerable computational effort of solving nonlinear equations to derive the switching angles, the large memory required to store the information for various modulation indexes, and the relatively sophisticated control to allow smooth transient pattern changes, are considered to be serious practical difficulties.

The other class is based on a certain low-frequency reference or modulating waveform, which is compared with a high frequency carrier waveform. These techniques are known as carrier PWM techniques, where the sinusoidal pulse-width modulation (SPWM) technique is the common one. It is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform [4].

Traditional analogue circuits rely on natural sampling techniques, where a fixed triangular carrier waveform is compared to a variable magnitude and frequency sinusoidal reference waveform. The intersection point determines the switching waveform. Digital designs provide improvements over their analogue counterparts. They are immune to noise and are less susceptible to voltage and temperature changes. Hence, a shift to digital implementation has been noted [4–7].

Development of the high performance microprocessor has encouraged work on digital PWM control. Implementation using the microprocessor was introduced in order to provide a more flexible method of designing the system. The system offers a simple circuitry, software control, and flexibility in adaptation to various applications. However, due to the high sampling rate required, it may limit the functionality of the processor to perform various tasks [7].

Generating PWM gating signals requires a high sampling rate in order to achieve a wide bandwidth performance. Therefore, most computation resources of a digital signal processor (DSP) of a microprocessor must be devoted to generating PWM signals. Segregation of task could be performed using a combination of microprocessor and DSP. A DSP chip handles the generation of PWM, while the processor feeds the information required by the DSP. Although this method could resolve the problem associated with sampling rate, it will complicate the design process [5].

FPGA is a programmable logic device (PLD) developed by Xilinx®, Inc. comprising thousands of logic gates. Some of them are combined to form a configurable logic block (CLB). A CLB simplifies higher-level circuit design. Interconnections between logic gates using software are defined through SRAM or ROM, which will provide flexibility in modifying the designed circuit without altering the hardware. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for complex circuitry and rapid prototyping make it the favourite choice for prototyping an application specific integrated circuit (ASIC). The advent of FPGA technology has enabled rapid prototyping of the digital system [8].

The flyback converter has a step-up and step-down characteristic, where the switching device controlled by a certain switching scheme plays an important part in its

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A.M. Omar is with the Electrical Engineering Dept., Faculty of Electrical Engineering, University Teknology MARA, Shah Alam, Selangor, 40450, Malaysia

N.A. Rahim is with the Electrical Engineering Dept., Faculty of Engineering, University Of Malaya, Kuala Lumpur 50603, Malaysia

function. However, when an AC supply is used in the converter system, the switching scheme must also consider the effect of generating harmonic currents and injection into the utility supply. Higher-order harmonics components could be filtered out using a conventional low pass LC filter, but the presence of low-order harmonics will increase the size of filter required.

Three-phase AC supply has been used as a source for the flyback converter system [9] and the converter has been designed to operate with less harmonic distortion on the AC supply. However, the system required memory chips to store the look-up table, and distributed to each gate driving circuit. The modulating signal was sampled and stored at 60°. Audible noise was present in the inductor due to the low number of carrier pulse used (12 pulses per half cycle). Adjustment on the power factor was not flexible and galvanic isolation was not considered.

To improve the above-mentioned idea for a three-phase system, this paper seeks to present the design of the three-phase PWM generator for a flyback converter using FPGA. A flyback converter has a special requirement during the turn-off period: the coil energy should be fully transferred into the load. The freewheeling current should be prevented from circulating in the bridge circuit. If this happens, it will reduce the energy that is being transferred to the load. To meet this requirement, a special PWM pattern needs to be designed. This paper introduces the steps and techniques for generating the three-phase PWM patterns for a flyback converter system, which is placed in one chip without using external memory chips.

2 Three-phase PWM switching scheme

The proposed three-phase PWM pattern is suitable for a flyback converter, with three devices-controlled bridge topology as shown in Fig. 1. The controller for generating PWM was designed for application specific integrated circuit (ASIC) technology. The ASIC used is made by Xilinx® and is called FPGA. The number of CLBs used in implementing the design is 169 and the number of input/output pins used is 17.

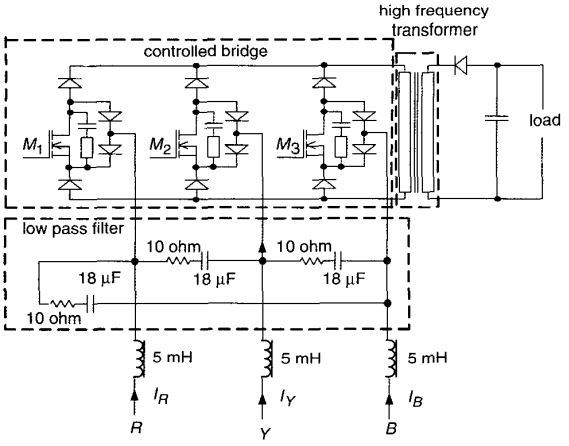

Fig. 1 *Flyback converter with three devices controlled bridge topology and isolation transformer*

A modified synchronous PWM is used for the PWM design. Two types of carrier are used, namely 'M' shape and 'W' shape. The two carrier signals will prevent the three PWM waveforms overlapping at the same time. The proposed concept for generating a three-phase PWM is

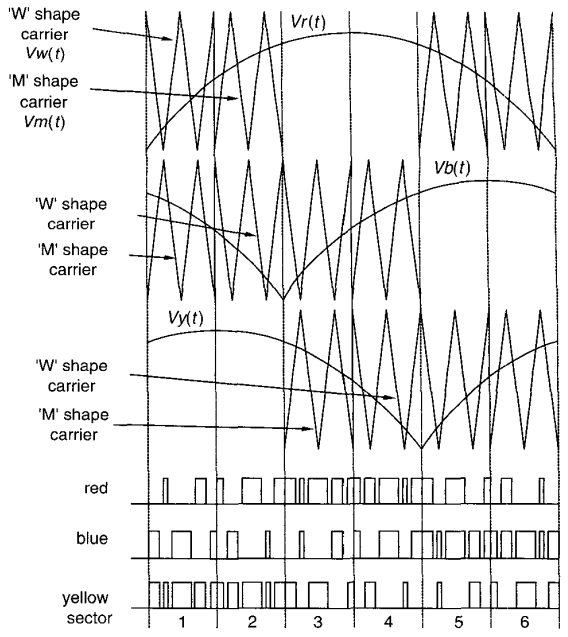

Fig. 2 *Method of generating three-phase PWM switching scheme*

shown in Fig. 2. A half cycle of single-phase waveforms is divided into six sectors, each sector consists of 30° angle. As an example for red phase PWM, in the first sector, the stored sample of red phase $Vr(t)$ is compared with the 'W' carrier $Vw(t)$. In the second sector $Vr(t)$ is compared with the 'M' carrier $Vm(t)$. The third and fourth sectors are a combination of the yellow and blue sectors. The fifth sector is similar to the second sector, and the last sector is similar to the first sector. The combination of sectors produced a symmetrical PWM pattern.

As an example, in the first sector, comparisons are based on the following conditions:

$$\begin{aligned} &\text{(i) If } Vr(t) \geq Vw(t), \text{ then Red} = 1 \\ &\text{(ii) If } Vr(t) < Vw(t), \text{ then Red} = 0 \end{aligned} \tag{1}$$

The 'W' carrier eliminates the long turn-off time of the red phase during zero crossing, which reduces the distortion on the output PWM produced. Similarly, the stored sample data of the blue phase $Vb(t)$ is compared with the 'M' shape carrier $Vm(t)$ to get the blue phase of the PWM pattern. The same conditions are applied to the blue phase:

$$\begin{aligned} &\text{(i) If } Vb(t) \geq Vm(t), \text{ then blue} = 1 \\ &\text{(ii) If } Vb(t) < Vm(t), \text{ then blue} = 0 \end{aligned} \tag{2}$$

Generation of the yellow phase PWM is derived using OR logic as,

$$\text{yellow} = \text{red or blue} \tag{3}$$

The PWM output patterns produced show that the switching operation depends on two states: (i) two phases are in the on-state (ii) all phases are in the off-state. This is very important in the flyback converter system because it prevents freewheeling current from circulating in the bridge circuit. Freewheeling current could reduce the amount of energy transfer to the load and also increase the power losses in the bridge circuit.

3 Modulator

One of the important elements in the FPGA design is the clock signal. The clock signal controls the carrier frequency as well as providing the clock signal for every module in the design and so must be calculated precisely. In this type of PWM design, only one main clock is required to clock the overall system. The carrier frequency *Fc* needs to be decided first in order to set the input clock frequency *F*clock. There are several factors that need to be considered before deciding on the carrier frequency: converter topology, type of power switching devices used and limitation of the peripheral components. The carrier frequency can be determined by:

$$Fc = F\text{clock}/[(2^n - 1) \times 2] \quad (4)$$

where *Fc* is the carrier frequency, *F*clock is the main clock frequency and *n* is the number of bits of the up–down counter. The main frequency clock, nominally set at 4.59 MHz, is locked to the AC mains frequency of 50 Hz by using a phase-locked loop circuit (PLL). By using (4), the carrier frequency is 9 kHz and suitable for circuit topology as in Fig. 1. Since the operating carrier frequency is not high, it has considerably less imposed switching stress on the power switching devices. By locking the clock frequency to the mains frequency, the modulating frequency of the bridge and the line frequency are synchronised. Therefore, there are no mains capture and synchronisation problems as the main supply frequency fluctuation tolerance is $\pm 2\%$. Fig. 3 shows the schematic of the phase-locked loop circuit.

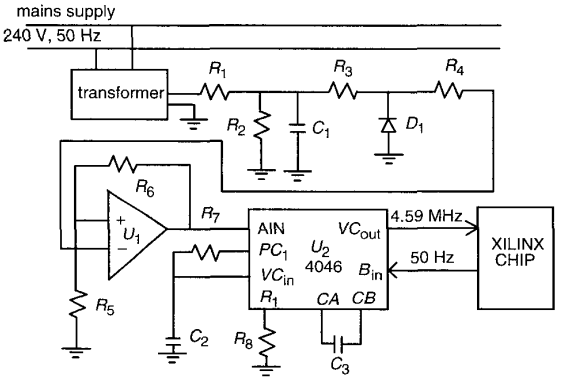

Fig. 3 *Phase locked-loop circuit*

The overall block diagram of the three-phase PWM modulator as developed in Xilinx FPGA is shown in Fig. 4. The design module consists of carrier, memory pointer, look-up table (ROM), multiplier, comparator, swapping, multiplexer, reset signal and OR logic function. The PWM gating signals are generated by comparing the scaled sine-wave reference signals with 'M shape' and 'W shape' carriers. An 8-bit up-down counter is used to generate the carrier waveform. The clock signal comes externally from the phase-locked loop circuitry. The data stored in the look-up table (internal ROM) consists of data from the red and blue phase only. A swapping unit and a multiplexer unit are used for selecting the required signals to the appropriate channel in order to form a proper PWM output pattern at the output terminals.

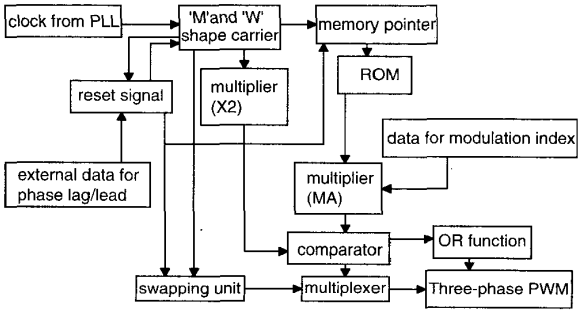

Fig. 4 *Overall block diagram of three-phase PWM modulator*

Shifting of PWM patterns is essential in order to vary the power factor of the system. It is carried out by delaying or advancing the reset signal, which is tied up with all the resettable modules. A positive triggering edge during a positive and negative cycle is used as a reference by the reset signal. Delaying or advancing the reset signal by the external command could force the current in the main circuit to lead or lag behind the voltage supply.

Division of the clock frequency from 4.59 MHz to 50 Hz is accomplished by using an internal counter in the Xilinx chip. The feedback frequency generated from the Xilinx chip is used as an input to the PLL chip, which locks and synchronises with the supply phase reference voltage.

4 Look-up table

The modulator uses a 30° sine wave look-up table, which is phase-locked to the AC line to generate a reference waveform. Two 30° patterns are stored in the look-up table, which is generated from the sine wave of the red and blue phases. Sixteen data from the red phase and 15 data from the blue phase were sampled and stored in the internal

Table 1

(*a*): Memory file for LogiBlox command for blue phase look up table

```
memfile COS. mem for LogiBLOX symbol MCOS
created on Sunday, November 08, 1998 16:08:52
header section
RADIX 10
DEPTH 128
WIDTH 8
DEFAULT 0
data section
specifies data to be stored in different addresses
RADIX 10
DATA 44,43,42,41,40,39,38,37,35,34,33,31,30,29,27,25
end of LogiBLOX memfile
```

(*b*) Memory file for LogiBlox command for red phase

```
memfile SIN.mem for LogiBLOX symbol mSIN
created on Sunday, November 08, 1998 16:28:48
header section
RADIX 10
DEPTH 128
WIDTH 8
DEFAULT 0
data section
RADIX 10
DATA 1,2,4,6,8,9,11,13,14,16,18,20,21,23,24
end of LogiBLOX memfile
```

ROM of the Xilinx chip. The samples were taken from 0° to 30° and 120° to 150°, respectively. Internal ROMs were created using the LogiBlox command, and the content of the memory files are shown in Table 1(*a*) and (*b*).

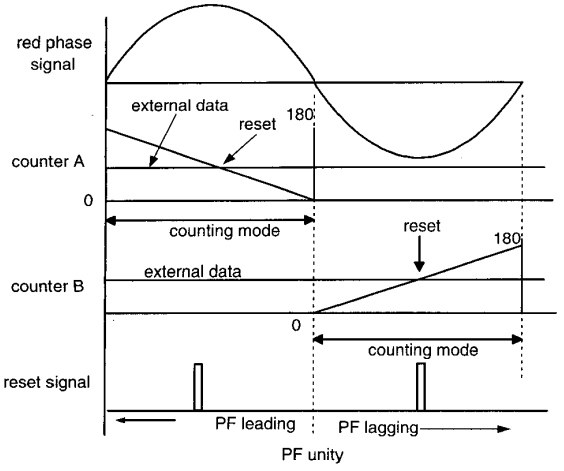

Fig. 5 *Operation of reset signal for phase shift*

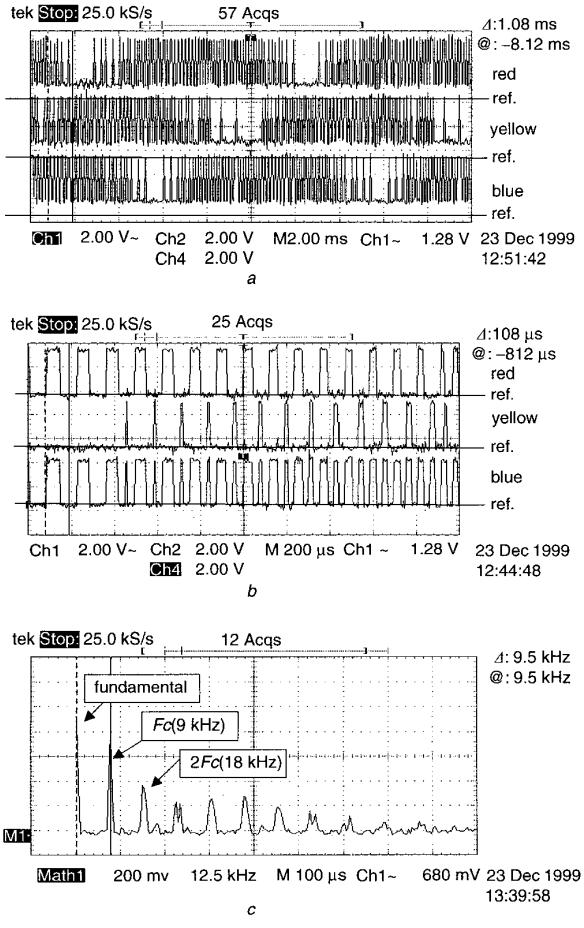

Fig. 6 *Three-phase PWM switching scheme at modulation index 0.5*
(*a*) Overall PWM pattern
(*b*) Enlarged scale of Fig. (a)
(*c*) Harmonic spectral of PWM pattern

5 Voltage and phase shift control

Voltage control is provided by changing the modulation depth of the PWM waveform. The per unit sample value from the look-up table is multiplied by the modulation index in order to generate the modulation waveform. The modulation waveform is then compared with the triangular carrier waveform to generate PWM patterns.

The phase shift is designed to provide flexibility in order to produce either lagging, leading or a unity displacement angle. Adjustment of power factors is accomplished by using an internal reset unit. Two eight-bit counters, two eight-bit comparators, a VHDL code block, a four-channel multiplexer and a few logic gates are used to form a reset unit. This unit is clocked from the signal derived from 'M' and 'W' shaped carrier units. During a positive cycle, counter A starts counting from 0 to 180. Fig. 5 shows the concept of controlling the phase shifter. During the counting process, the comparator compares the counter value with the external input data. If the values are equal, it produces a pulse output signal. The pulse will reset all the modules and the PWM patterns restart. Thus, this signal determines the lagging phase shift. Similarly, for a negative cycle, counter B starts counting, and the comparator compares the counter value with the external data. If the values are equal, it produces a pulse output signal that will reset all modules. This signal determines the leading phase shift. If the external data is set at 180, the PWM waveforms become the same phase as the reference voltage (i.e. unity power factor). However, for three devices bridge topology as in Fig. 1, the actual phase shift could be varied from −30° to 30°. The external data for a phase shift angle may come from a personal computer or from any feedback controller unit.

6 Experimental results

Validity of the ASIC design of the synchronous PWM for the three-phase flyback converter has been verified experi-

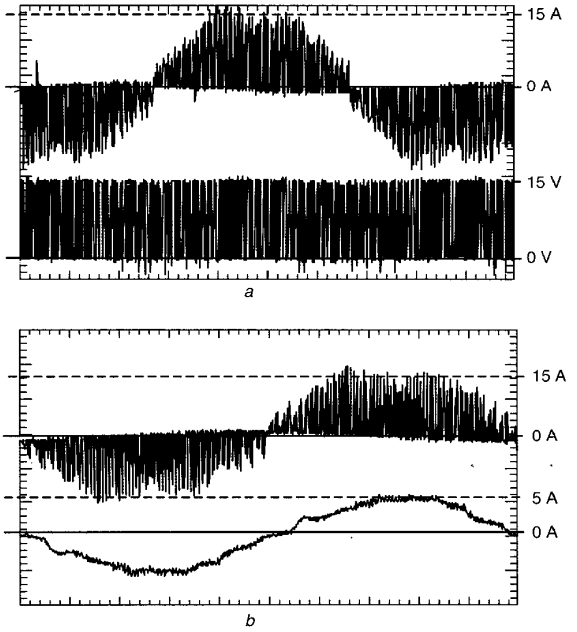

Fig. 7 *AC current at modulation index 0.5*
(*a*) *Bottom*: PWM switching pattern from driving circuit *Top*: Unfiltered AC current
(*b*) *Bottom*: Filtered AC current *Top*: Unfiltered AC current

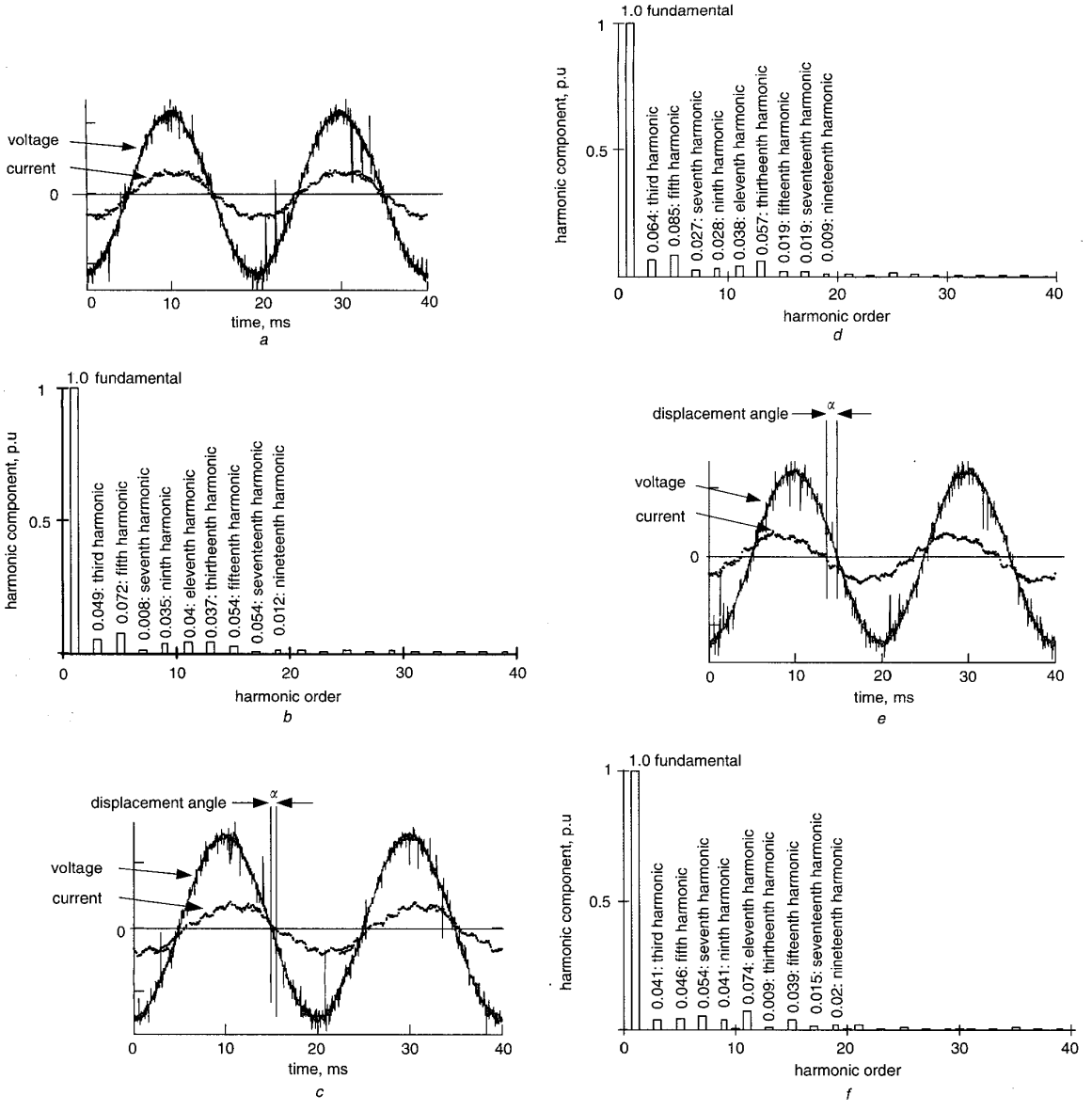

Fig. 8 *Effect of shifting PWM pattern on operating power factor*
(*a*) Current and voltage waveform at unity power factor
(*b*) Harmonic current spectral at unity power factor
(*c*) Current and voltage waveform at lagging power factor
(*d*) Harmonic current spectral at lagging power factor
(*e*) Current and voltage waveform at leading power factor
(*f*) Harmonic current spectral at leading power factor

mentally on a prototype system. The software XACT STEP M1 of the foundation series has been used to convert the schematic entry level to an appropriate bit file prior to download into the Xilinx XC4005E chip.

During testing, the clock signal from the phase-locked loop circuit is running at 4.59 MHz. The three-phase PWM patterns produced are shown in Fig. 6(*a*). The enlarged scale of Fig. 6(*a*) is shown in Fig. 6(*b*). The Figure shows that only two signals are in a high state at any one time and this condition is essential for flyback converter as has been discussed earlier. Although the PWM patterns shown are suitable for driving a bridge circuit with a three-power switching device topology (Fig. 1), the pattern could be separated into positive and negative cycles for operation with the conventional six devices bridge topology.

The harmonics spectrum of the PWM pattern produced is shown in Fig. 6(*c*). The fundamental component has the highest magnitude. As expected, the carrier frequency of 9 kHz and its multiple frequencies are present in the waveform.

The effect of PWM switching on the AC current is shown in Fig. 7(*a*). The AC current pulses obtained consist of fundamental and harmonic components. The harmonic components are filtered out using low-pass LC filters and the result is shown in Fig. 7(*b*).

The flexibility of shifting the PWM patterns either in phase, lagging or leading with the reference voltage signal could force the system to operate on those modes as demonstrated in Fig. 8(*a*), (*c*) and (*e*), respectively. The Figures also show that the filtered AC current injected back into the AC power supply is nearly sinusoidal in shape, with

a total harmonic distortion (THD) of 11.12%. Small amounts of harmonic components still exist in the current waveforms, as shown in the frequency spectrum in Fig. 8(*b*), (*d*) and (*f*). At a unity power factor operating mode, the fifth harmonic contributes the highest harmonic component. The Figures also show that the levels of harmonic components change as the operating mode changes.

The cut-off frequency of the low-pass filter is sufficiently low for the resonant frequency to be very much lower than the switching frequency. This could prevent current oscillation.

7 Conclusions

A compact three-phase PWM generator suitable for the three-phase Flyback converter system has been developed and tested successfully. PWM design is placed on a single chip of XC4005E FPGA and is capable of providing flexibility in order to produce the PWM pattern either same phase, lagging or leading the reference voltage signal. The overall system is compact with no external memory system required. Tests have been carried out to show the effectiveness and flexibility of the proposed method.

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