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Generalized Selective Harmonic Elimination Modulation for Transistor-Clamped H-Bridge Multilevel Inverter

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Abstract

This paper presents a simple approach for the selective harmonic elimination (SHE) of multilevel inverter based on the transistor-clamped H-bridge (TCHB) family. The SHE modulation is derived from the sinusoidal voltage-angle equal criteria corresponding to the optimized switching angles. The switching angles are computed offline by solving transcendental non-linear equations characterizing the harmonic contents using the Newton-Raphson method to produce an optimum stepped output. Simulation and experimental tests are conducted for verification of the analytical solutions. An Altera DE2 field-programmable gate array (FPGA) board is used as the digital controller device in order to verify the proposed SHE modulation in real-time applications. An analysis of the voltage total harmonic distortion (THD) has been obtained for multiple output voltage cases. In terms of the THD, the results showed that the higher the number of output levels, the lower the THD due to an increase number of harmonic orders being eliminated.

Key words: Harmonic elimination, Multilevel inverter, Pulse-width modulation (PWM), Single-phase inverter, Total harmonic distortion (THD)

I. INTRODUCTION

Recently, the demand for medium-voltage, higher power converters that are capable of producing high quality waveforms, while utilizing low voltage devices and reduced switching frequencies have led to increases in multilevel inverter development. Over the years, several multilevel inverter topologies have been developed as alternatives for medium voltage and high power applications, and they offer advantages over the single switch and series connection approaches [1]. Multilevel inverters have been shown to have the following advantages: reduce common-mode voltage, lower switching stress, lower total harmonic distortion (THD), improve output voltage/current quality, etc. [2]-[4].

The most common multilevel inverter topologies include the diode clamped or neutral point clamped (NPC), capacitor clamped or flying capacitor (FC), and cascaded H-bridge (CHB) inverters [3]-[8]. It is absolutely necessary to produce an effective and innovative power converter design, from the perspective of cost and efficiency, for optimizing output power with significantly fewer losses. The requirements for the maximum voltage and current total harmonic distortions (THDs), as specified in IEEE Std.519-1992, must be fulfilled by the multilevel inverter [9]. Some researchers have overcome the complexity of the multilevel inverter circuit by rearranging the switches and DC voltage sources [10]. This produces a new breed of multilevel topologies: the active NPC (ANPC) [11], modular multilevel converter (MMC) [12] and transistor-clamped converter (TCC) [13], [14].

To obtain a good output voltage, various modulation algorithms have been developed for multilevel inverters. They are classified according to their switching frequency. Each has

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